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PROCEEDINGS OF THE 13th WORKSHOP ON COMPOUND SEMICONDUCTOR DEVICES AND INTEGRATED CIRCUITS HELD IN EUROPE

CABOURG, France, May 10th to 12th 1989

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Technische Hochschule Darmstadt, FRG.

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AEG, Ulm, FRG

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Technical University of Aachen - Aixtron, FRG.

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Duisburg U., FRG.

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Michigan U., USA.

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F. Eisen
Fraunhofer Institut, Freiburg, FRG

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CNET, Lannion, France.

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Technical University of Darmstadt, FRG.

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A. Ehrenheim, F. Vidimari
Telettra, Italy

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Aachen Technical University.

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Ecole Centrale de Lyon, France.

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D. Pavlidis, K. Tomizawa and D. Pehlke
The University of Michigan, Ann Arbor, USA.

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Technical University of Munich, FRG.

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A. Oulismani, H. Hafidallah, G. Vernet and R. Adde

Institut d'électronique fondamentale, Orsay, France.

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Siemens, München, FRG.

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Alcatel/SEL, Stuttgart, FRG.

A. Technology for mm wave receiver components

G. Ebert, J. Selders and A. Colquhoun

Telefunken, Heilbronn, FRG

INVITED PAPERS

Large Area MOCVD for Opto-microwave Electronic Components.

Invited : A. MIRCEA, CNET Bagneux, France.

Temperature Limitations of GaAs Power Devices.

Invited : H. Hartnagel, Technische Hochschule Darmstadt, FRG.

Temperature Limitation of GaAs Power Devices

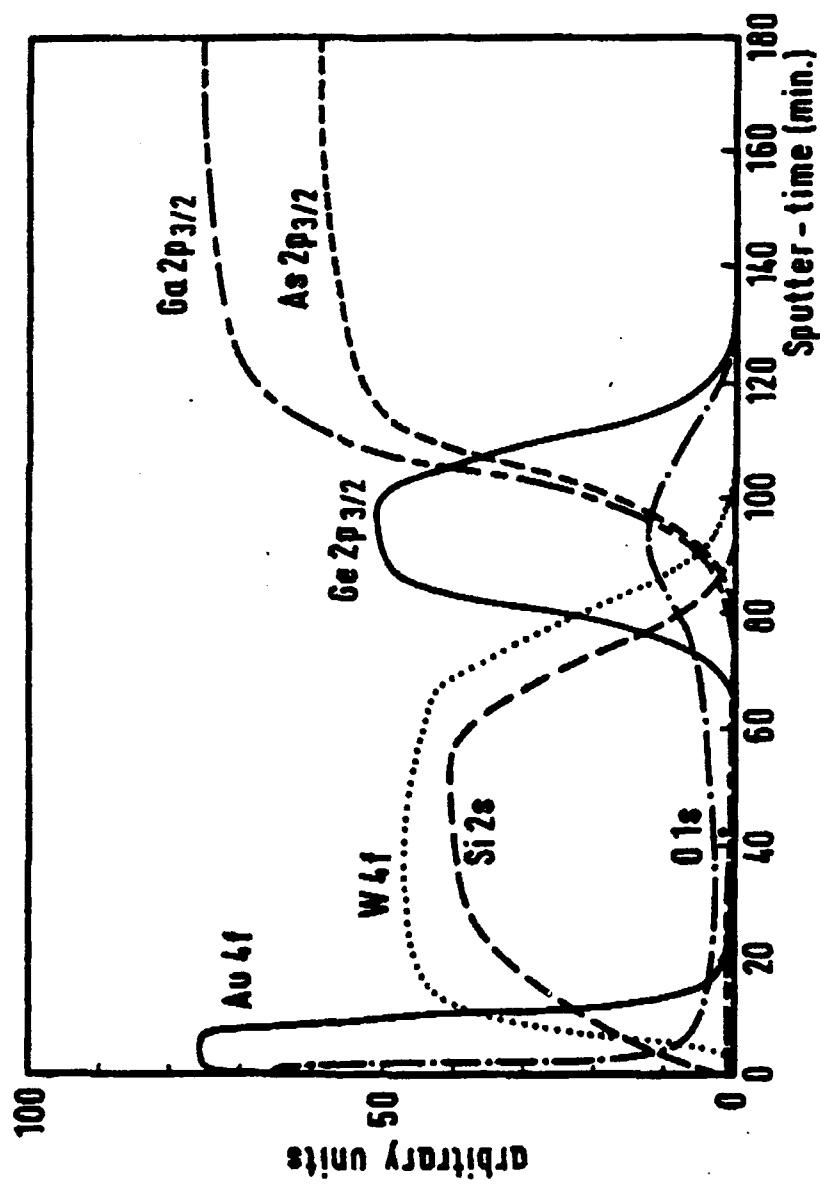
H. L. Hartnagel
Institut für Hochfrequenztechnik
Technische Hochschule
Merckstraße 25
D-6100 Darmstadt
F. R. Germany

With the limited efficiencies of power devices, heat dissipation and the resulting temperature increase, usually limits power handling capabilities particularly with the relatively small heat conductivity of GaAs. However, leakage current of GaAs devices are lower at increased temperatures than those of Si due to the larger energy gaps. It is therefore useful to evaluate the other performance-limiting changes of device parameters when temperatures are increased. There are firstly the irreversible processes of a) the formation of a conductive layer on free surfaces of GaAs, possibly by the evaporation, or by selective oxidation of As, leaving metallic Ga clusters and b) the interdiffusive deterioration of metal contacts on GaAs, particularly associated with Au. Total IC or device coverage of Si_3N_4 by a suitable low-temperature plasma deposition process stabilizes the surface. Systematic testing of adhesion properties are then required (Fig. 1 + 2). Metallic contacts need to be improved using diffusion barrier systems so that the outdiffusion of Ga and the indiffusion of Au from a top layer (which is useful for low-resistivity metallizations) is avoided. Suitably deposited WSi_n together with an intermediate Ti layer (which possibly acts as grain-boundary blocking material) has been found very suitable (Fig. 3), but other sandwiches are also of interest. If these aspects of a high-operating-temperature device technology are systematically introduced, the devices are found to work over long periods even at temperatures of 400°C (see paper at this workshop by Schweeger et al. regarding the related field of "High Temperature Electronics").

Then, however, reversible effects cause a deterioration of device performance at increased operating temperatures. The mobility and the saturation velocity of electrons are reduced. This means a reduction in transconductance

and of the maximal current of the n channel of field effect transistors. It also means that some sensor performances are affected such as the output signal in Hall sensors. On the other hand pressure sensing due to the piezo-electric properties of GaAs are still possible (to be published by Fricke et al shortly). Other device areas concern light emitters (led and laser), where only little information is available still on the question where there is the fundamental temperature limitation of light emission from electron-hole recombination.

XPS-SPUTTER - PROFILE



GaAs - Ge - WSi₂ - Au (annealed at 460°C for 60 minutes)

Fig. 3

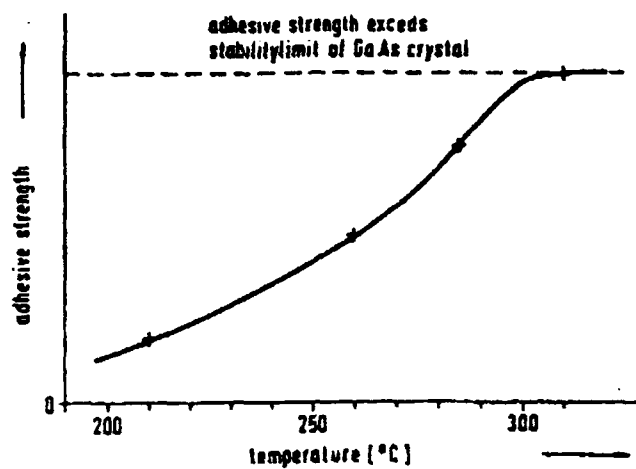


Fig. 2

Adhesive strength as a function of sample-holder temperature during the PECV-deposition

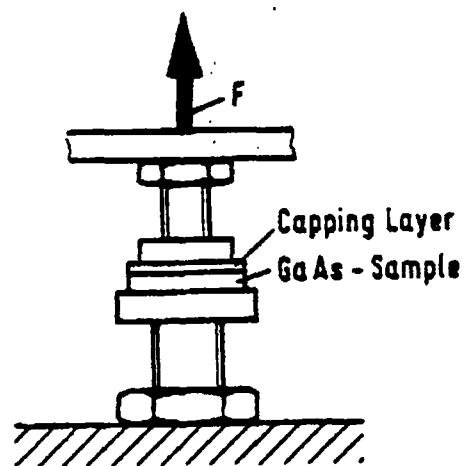


Fig. 1

Test rig for adhesion measurements

Some Circuit Applications of HBT's

Invited : P. Topham, Plessey Research Ltd, England.

CIRCUIT APPLICATIONS OF HETEROJUNCTION BIPOLAR TRANSISTORS

P.J.Topham

Plessey Research Caswell Ltd
Allen Clark Research Centre
Towcester, Northants, England

The aim of this paper is to show the application of GaAs/GaAlAs Heterojunction Bipolar Transistors (HBT) to a range of circuits which can be used in telecommunications systems.

We have developed an ion implanted HBT process based on material grown by atmospheric pressure MOCVD. Transistors produced by this process have a current gain transition frequency (f_T) of 40GHz. These transistors have been used to produce a range of wide band gain blocks. Versions have been produced with DC to 5GHz bandwidths (at -3dB) and also with 18dBm output at 1dB gain compression. These gain blocks have been used to drive laser diodes at a data rate of 2Gbit/s.

The same process has also been used to make an ECL/CML gate array. This has 144 equivalent gates and 8 high speed differential input/output ports. The array has been customised as dividers, multiplexers and demultiplexers. The gate array divide-by-eight circuits have been clocked at 3.2GHz. This array also gives a useful guide to the yield of the process, with 55% of multiplexers functional at wafer probe.

This work shows that a high yield HBT process has been developed using ion implanted MOCVD material. The ability to make wideband analogue circuits and high speed MSI circuits on the same process opens up many applications for the HBT.

Heterojunction Engineering Devices-Quantum-Mechanical Effect

Devices : Current Status in Japan.

Invited : N. Yokoyama, Fujitsu laboratories Ltd, Japan.

Heterojunction Engineering Devices--Quantum-Mechanical Effect Devices: Current Status in Japan

Invited: Naoki Yokoyama, *Fujitsu Laboratories Ltd.*, Morinosato, Atsugi 243-01, Japan

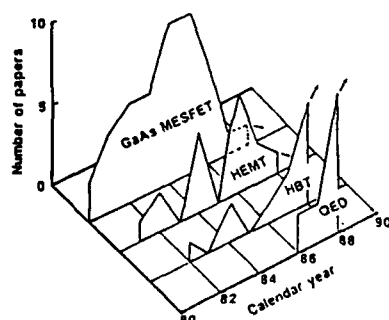
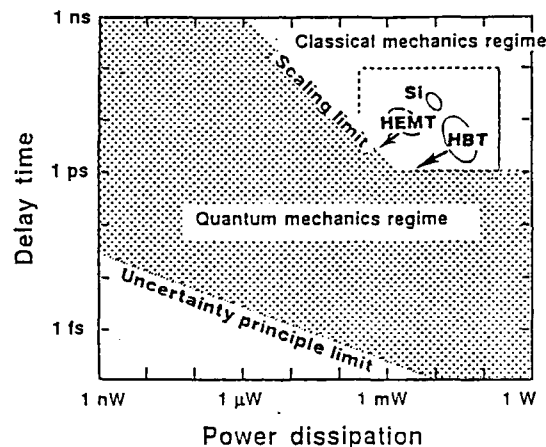
Recently, the interest of Japanese researchers in compound semiconductor devices seems to have switched to the development of new electron devices. They recognize that there is a scaling limitation in conventional semiconductor devices due to quantum-mechanical effects such as tunneling and size quantization. Since conventional devices use the particle-like nature of electrons, they meet a scaling limit caused by the wave-like nature of electrons. The solution to breaking this barrier is to develop devices using the wave-like nature of electrons positively. In fact, the number of papers relating to quantum-mechanical effect devices, reported at the Conference on Solid-State Devices and Materials SSDM in Japan, increased rapidly. The number of papers relating to GaAs MESFET and HEMT has decreased, however.

The resonant-tunneling hot electron transistor (RHET) proposed by us in 1985 is a quantum mechanical effect device, because the resonant-tunneling effects come from the wave-like nature of electrons. The RHET, recently fabricated using an InAlAs/InGaAs pseudomorphic resonant-tunneling emitter exhibited improved DC performance. The microwave performance was measured for the RHET, and an f_T of 63 GHz and an f_{max} of 44 GHz were obtained at 62K. Using RHET-equivalent circuit analysis, we estimated the response time of the resonant-tunneling barrier to be short, at 0.47 ps. The collector transit time is rather long at around 1 ps due to intervalley scattering in the collector barrier. With decreased thickness of the collector barrier, a cutoff frequency over 100 GHz is possible. The switching speed of the RHET should be comparable to that of the HBT, with decreased power dissipation. Memory and logic circuits can also be built using RHETs with a reduced number of devices, making the RHET a candidate for devices to be used in the next decade.

Aharonov-Bohm effects in ultrafine GaAs/AlGaAs 2DEG rings, fabricated using EB microfabrication, were first observed by Ishibashi of Osaka University. To develop quantum interference devices using the electrostatic AB effects proposed by Datta of Purdue University, we need to make single-mode electron waves with an increased coherent length. This is done by making quantum wires. Sakaki of the University of Tokyo reported the possibility of elastic scattering suppression in ultrafine semiconductor wires (quantum wires) in 1980. More recently (February 1989), he proposed the possibility of reduced optical phonon scattering in quantum wires having a periodic potential structure. These scattering suppressions may increase the coherent length of electrons. In 1988, we fabricated HEMTs using quantum wires. The oscillatory characteristics in HEMT transconductance, possibly due to electron mobility modulation caused by quantum size effects, were observed. Ikoma's group at the University of Tokyo has made the quantum wire HEMT using FIB techniques and observed oscillatory characteristics in transconductance. However, they claim that the oscillatory characteristics are not due to mobility modulation. The coherent length of electron waves in ultrafine GaAs bulk and the high-mobility electron gas confined in the HEMT structure with FIB implantation were studied by the same group. Electron-electron scattering seems to break electron coherency at around 4.2K. Basic research on the mechanism to break electron coherency is expected to continue.

The intriguing characteristics of superlattice devices come from the interference effects of electrons with periodic potentials. Superlattice devices fall into two categories--vertical superlattice devices proposed by Esaki in 1970 and the lateral superlattice devices proposed by Sakaki in 1975. The latter is now being studied in Japan. Fukui et al. of NTT developed an MOCVD technique to make lateral superlattices using misoriented GaAs wafers. They also fabricated an improved washboard transistor and velocity modulation transistor using lateral superlattices embedded in semiconductors. Diffraction is another important nature of waves. Furuya of the Tokyo Institute of Technology proposed electron diffraction devices using gatings embedded in semiconductors. The use of lateral superlattices will make possible the diffraction transistor.

Thus, compound semiconductor researchers in Japan seem to be focusing on quantum-mechanical effect devices and the physics involved. It is not clear whether these devices will become useful, but these devices will clearly appeal to researchers' curiosity.



Trends of Papers at SSDM in Japan

Quantum-Mechanical Effect Devices

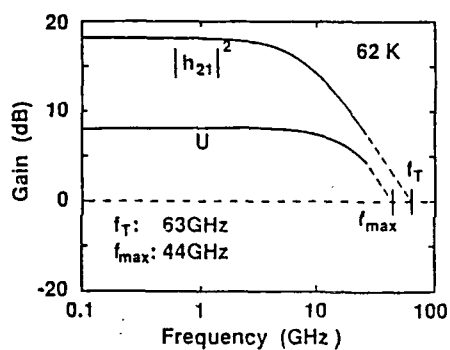
□ Use of wave-like nature of electrons

- Fabry-Perot Interferometer
 - Resonant-tunneling devices
- Mach-Zehnder Interferometer
 - AB effect devices
- Interference filter
 - Superlattice devices
- Diffraction grating
 - Electron diffraction devices

Energy band diagram of a GaAs/AlGaAs heterostructure. The diagram shows energy levels (E) on the y-axis and position on the x-axis. It features an InGaAs well (4.1 nm) and an InAlAs barrier (2.6 nm). The InGaAs well is 30 nm wide, and the InAlGaAs barrier is 200 nm wide. The energy levels are labeled A, B, and C. The InGaAs well is labeled "InGaAs 30 nm" and the InAlGaAs barrier is labeled "InAlGaAs 200 nm". The energy levels are labeled "InGaAs", "InAlAs barrier (2.6 nm)", "InGaAs well (4.1 nm)", "InGaAs 30 nm", "InAlGaAs 200 nm", and "InGaAs".

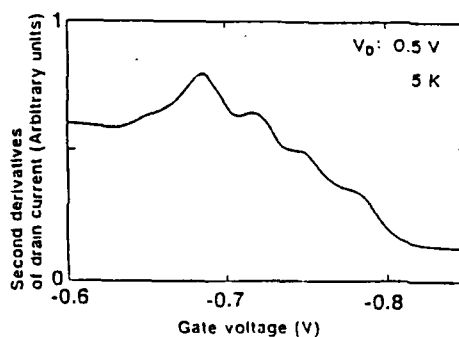
Chemical formulas for the materials are provided below the diagram:

- InGaAs: $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$
- InAlAs: $\text{In}_{0.35}\text{Al}_{0.65}\text{As}$



The diagram illustrates the operation of a quantum dot (QD) as a single electron transistor. The left part shows a QD with a gate voltage applied, creating a Coulomb diamond in the differential conductance (dI/dV) as a function of gate voltage (V_g). The right part shows the energy levels of the QD, with a single electron (e^-) occupying the lowest energy state, labeled "Single mode".

The figure contains two schematic cross-sectional diagrams of semiconductor structures. The left diagram, labeled '2DEG' at the bottom, shows a stack of layers: a bottom 'i-GaAs' layer, an 'n-AlGaAs' layer, and a top 'n-GaAs' layer. An 'Al gate' is shown on the surface of the n-GaAs layer, connected to ground. The right diagram, labeled '1DEG (Quantum wires)' at the bottom, shows a similar stack of 'i-GaAs' and 'n-AlGaAs' layers. The top 'n-GaAs' layer is thinner and has a 'Depletion layer' indicated below it. An 'Al gate' is also present on the surface, but it is connected to a negative voltage source labeled '-V_G'.



Circuit Applications of Self-aligned Heterojunction Bipolar Transistors.

Invited : K. Honjo, NEC Corporation, Japan.

Circuit applications of self-aligned heterojunction
bipolar transistors

Kazuhiko HONJO
(NEC Corporation)

This paper describes circuit applications of self-aligned HBTs. Typical features for HBTs are (1) high transconductance g_m , (2) low threshold voltage variation, (3) high f_t and f_{max} , (4) low $1/f$ noise.

Taking these advantages into consideration, two major application fields can be considered. One is a microwave and millimeter wave low phase noise oscillator application. The other is a LSI application having heavy loads such as gate array circuits. For both applications, development of the self-aligned HBT process is a key.

First, a side wall assisted fully self-aligned process and a pattern inversion self-aligned process developed by NEC are described.

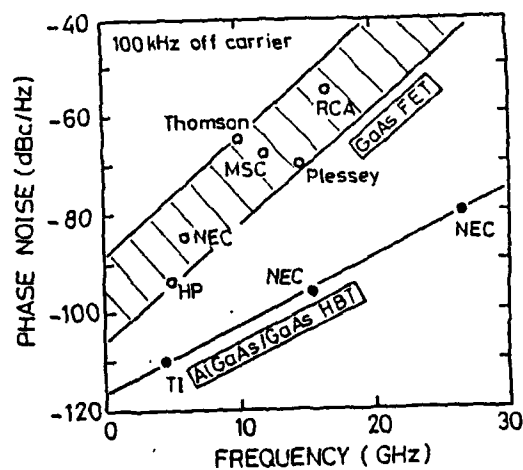
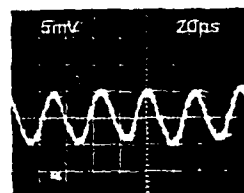
Using the self-aligned HBT, a low phase noise 28 GHz band oscillator has been developed. Under a free running condition, phase noise of -80 dBc/Hz at 100 kHz off carrier could be achieved. The phase noise value is 20-30 dB superior to the phase noise of GaAs FET oscillators.

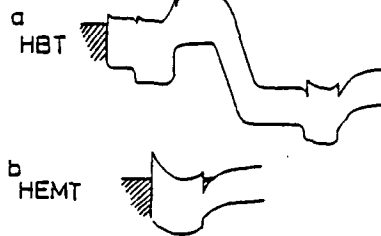
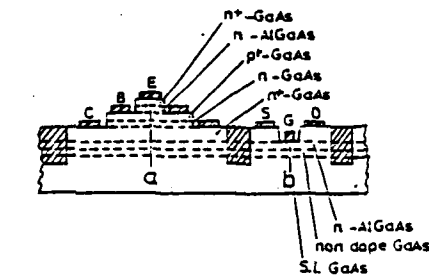
It is concluded that in microwave and millimeter wave ranges, HBT is suitable for oscillators, beside HEMT is effective for amplification. Co-integration of HBT and HEMT on a single GaAs chip will also be mentioned at the workshop.

For digital circuit applications, we obtained ring oscillator $t_{pd}=9.5$ ps with 13 mW (CML) and $t_{pd}=16.7$ ps with 4 mW (ECL) using the fully self-aligned HBTs. Power delay product of our device, $6.7E-14$ J, for ECL, is the lowest value ever reported for HBTs.

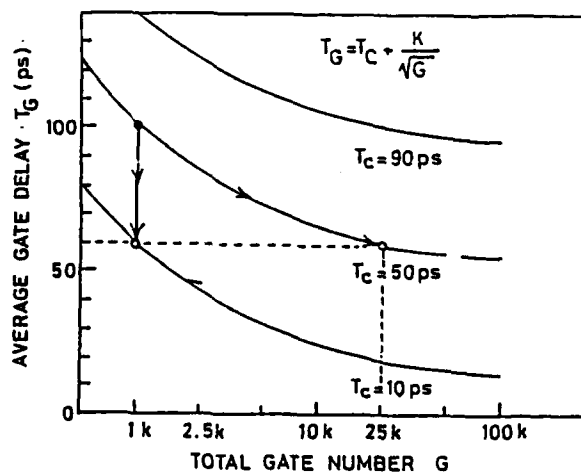
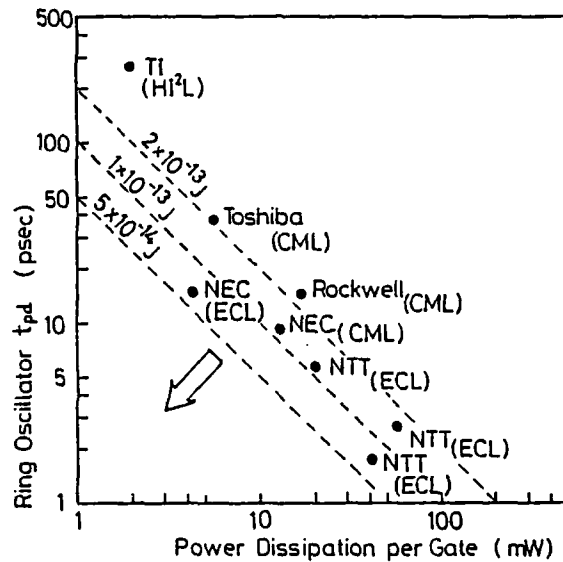
Based on the results, we simulated gate array performance using SPICE. Under a condition of $F1=F0=3$, $l=3\mu m$, which is a standard condition for LSIs, delay time can be estimated as 70 ps. Note that propagation time

A schematic diagram of a cross-section of a gas turbine engine component, likely a combustor or turbine inlet guide vane. The diagram shows a central core (E) surrounded by a SiO₂ layer. The side walls are labeled SiO₂ SIDE WALLS. The base is labeled C and H₂O. The bottom layer is labeled B-GAS, A-GAS, and S.I. GAS. The top layer is labeled C and H₂O.

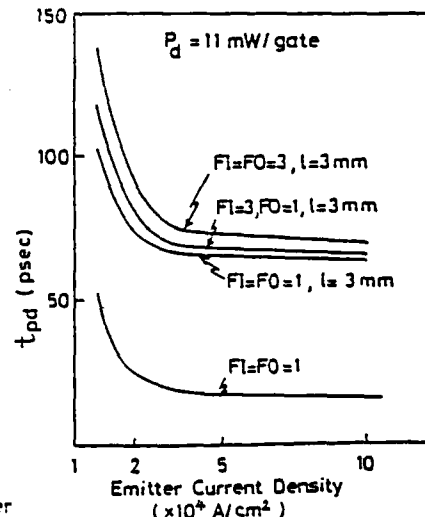




Co-integration of HBT and HEMT without using selective epitaxy



Reduction of average gate delay by increasing total gate number



HBT ECL gate propagation delay for different load condition

Optimization of MODFET Structures for High Performance.

Invited : L. Eastman, Cornell University, USA.

Optimization of MODFET Structures for High Performance

Lester F. Eastman

School of Electrical Engineering and National Nanofabrication Facility

Cornell University, Phillips Hall, Ithaca, NY 14853 USA

Short gate heterojunction field effect transistors, grown by MBE on GaAs and InP substrates have yielded excellent performance at high frequency. The conduction band potential step must be maximized in such MODFET structures in order to have a large two-dimensional-electron-gas (2DEG). On GaAs substrates, pseudomorphic, or strained, quantum wells have been used to reach potential steps over .40V. These use $\text{In}_y\text{Ga}_{1-y}\text{As}$ quantum wells with $y = .25$ and thickness of $\sim 100 \text{ \AA}$. The barrier layer is $\text{Al}_x\text{Ga}_{1-x}\text{As}$ with $.22 \leq x \leq .30$ and is heavily doped in a thin layer with only a small spacer layer. Figure 1 shows the conduction band profile for such a MODFET with either GaAs or $\text{In}_{.15}\text{Ga}_{.85}\text{As}$ active channel. The $\text{In}_{.25}\text{Ga}_{.75}\text{As}$ channels were optimized with 50 \AA spacer layers, rather than 25 \AA . In the latter case, the electron sheet density in the 2DEG was maximized at $2.4 \times 10^{12}/\text{cm}^2$. Figure 2 shows that the thickness of the quantum well is optimized at $\sim 100 \text{ \AA}$ for $y = .25$, and Figure 3 shows the microwave performance of such a device. The 152 GHz result of Dr. Loi Nguyen, using wafers grown by Dr. David Radulescu is the present state of the art on GaAs substrates. This device has 150 \mu m gate width in order to minimize the leading effects of the probe pad capacitance. For a 50 \mu m width, the devices gave 112 GHz f_T and 250 GHz f_{max} , with larger fractional capacitance loading. In integrated circuits, the full intrinsic f_T of $\sim 180 \text{ GHz}$ is available, as well as the high f_{max} . Figure 4 shows all the results for f_T , vs gate length, from various

laboratories. For the GaAs channel, with $y = 0$, the use of atomic planar doping enhances results, since the conduction band potential step is only .24V for that case. The average electron transit velocity is 1.2 - 1.3 for $y = 0$, is 1.5 for $y = .15$, and for $y = .25$ is about 1.8×10^7 cm/s. No strong evidence for velocity overshoot is seen down to gate lengths of .10 μm .

Using InP substrates with $\text{Al}_{.48}\text{In}_{.52}\text{As}$ barriers and $\text{Ga}_{.47}\text{In}_{.53}\text{As}$ channels, even higher performance is possible. Figure 5 shows the cross section of a device fabricated by Dr. Lauren Palmateer, from a wafer grown by MBE by Dr. William Schaff. Tri-level resist is used during electron beam lithography to form the gate of this device, as was also the case for the previous device. Using optimized MBE growth conditions, traps in the AlInAs were minimized, so that the kink effect in I(V) curves was minimized. Figure 6 shows the microwave measurement of current gain for a device with .1 x 100 μm gate width. In these MODFET devices on InP the average electron transit time was near 2.4×10^7 cm/s.

In all cases the measurements were made with coplanar waveguide triple probes (Cascade Company) and these measurements were used by Dr. Paul Tasker to set up models for the equivalent circuit elements and the corresponding physical electronics phenomena. A detailed simulation of the 2DEG using Schroedinger and Poisson equations, has also been made by Dr. Mark Foisy. Using $y \approx .65$, Drs. April Brown and Umesh Mishra of Hughes Research Laboratory have obtained 210 GHz f_T values with a .1 μm x 200 μm gate device. They also got .8 dB noise figure at 60 GHz with a .2 μm lattice-matched device.

Figure 7 and 8 show all of the state of the art results for GaAs and InP substrates. Of special note is the HBT results of Drs. R. Nottenberg, Y.K. Chen, and M. Panish of AT &T Bell Laboratory, reaching 244 GHz f_T at 77 GHz, the highest ever gotten with any transistor to date.

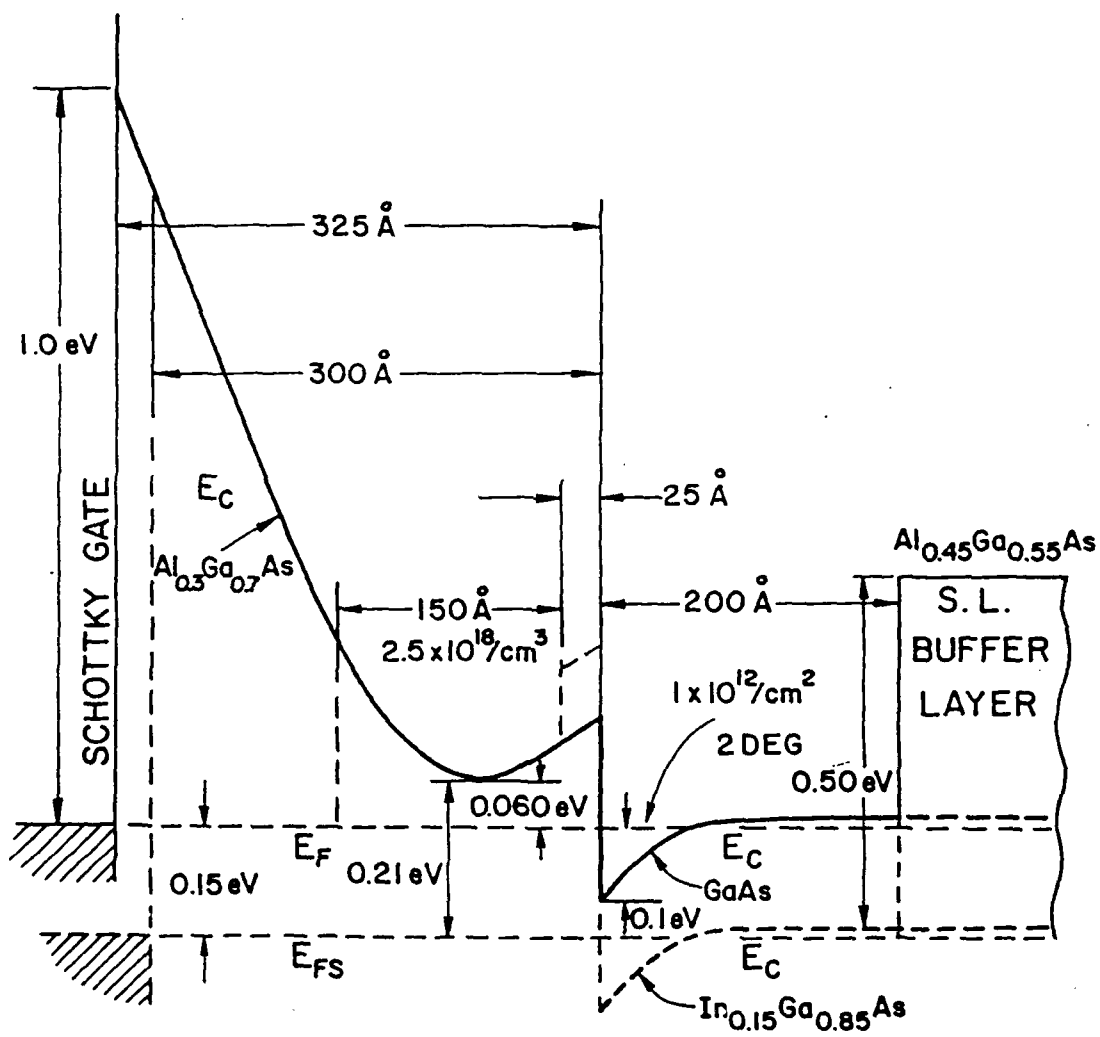


FIGURE 1

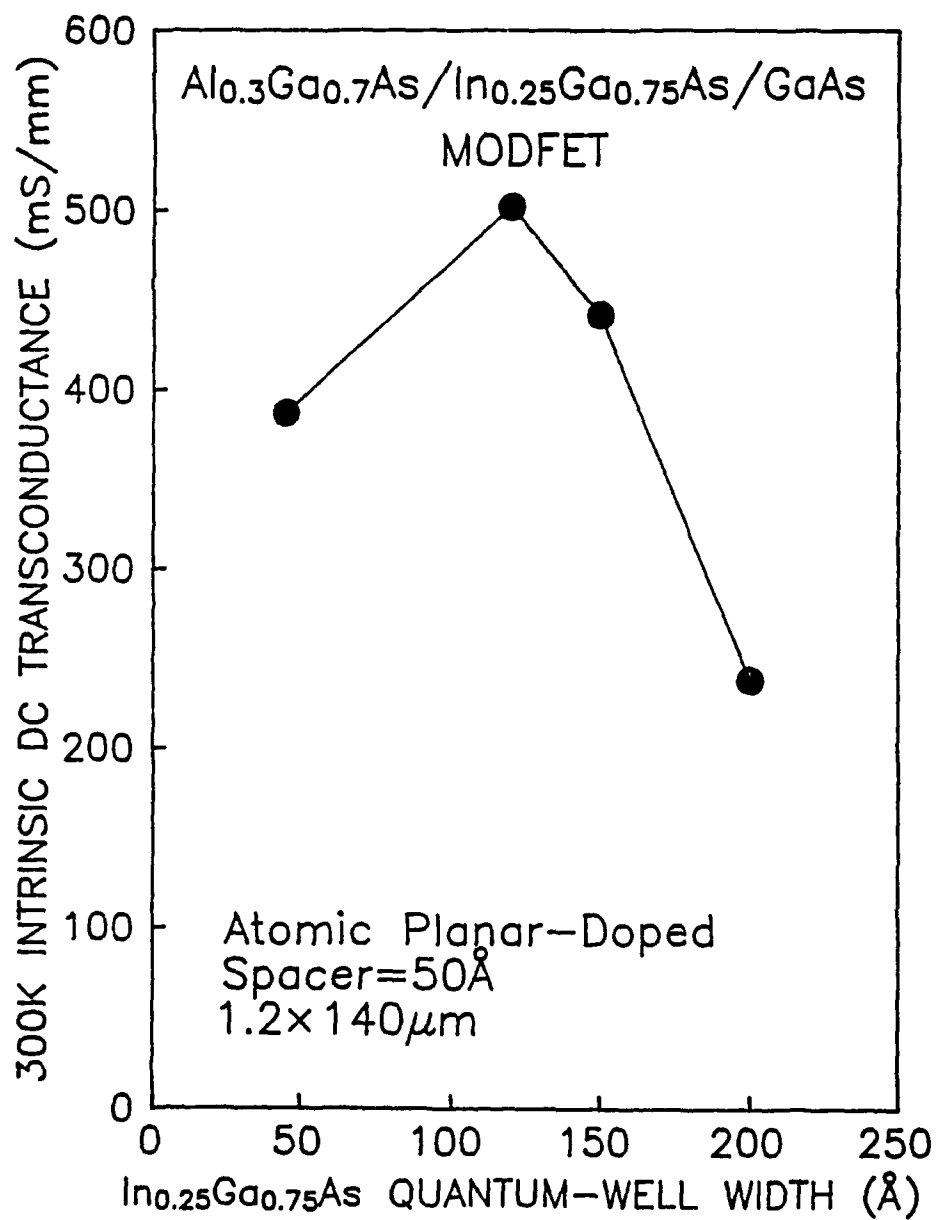


FIGURE 2

0.15X150 μ m MUSHROOM GATE InGaAs MODFET

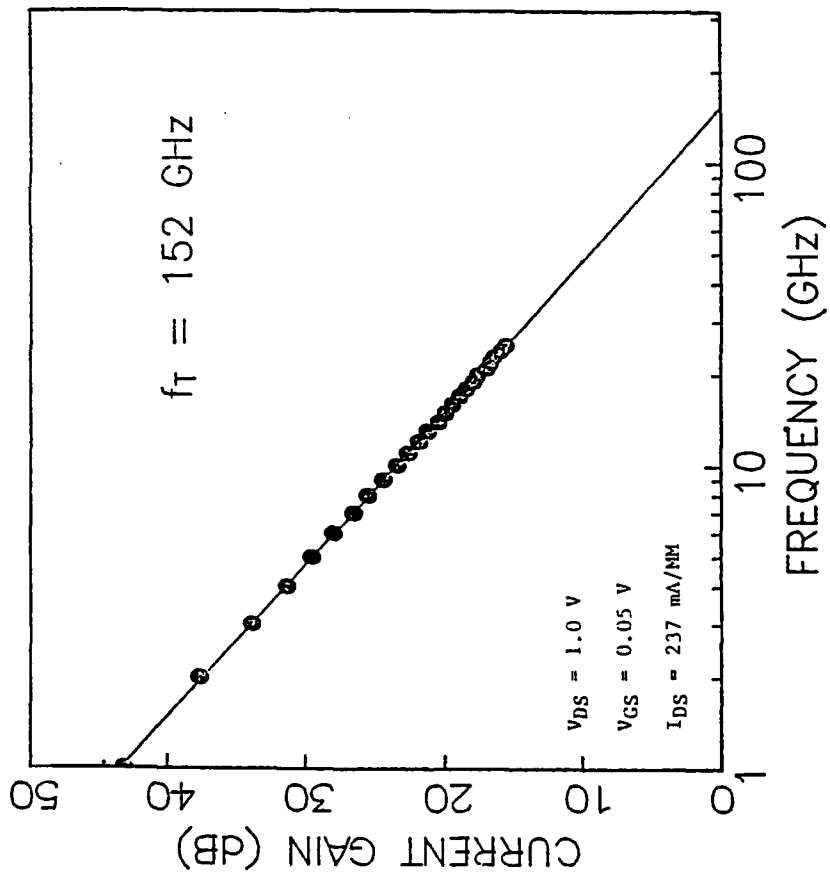


FIGURE 3

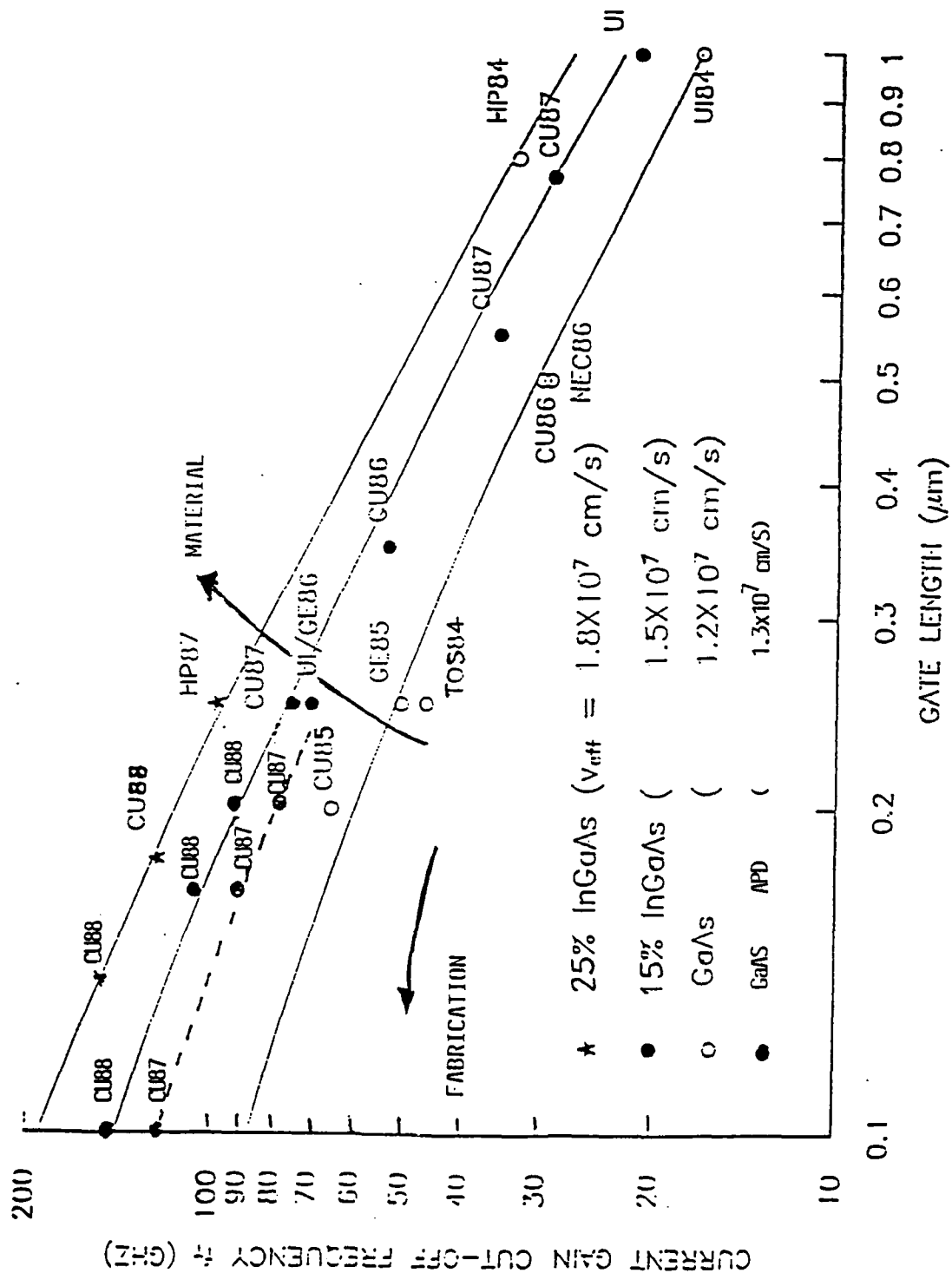
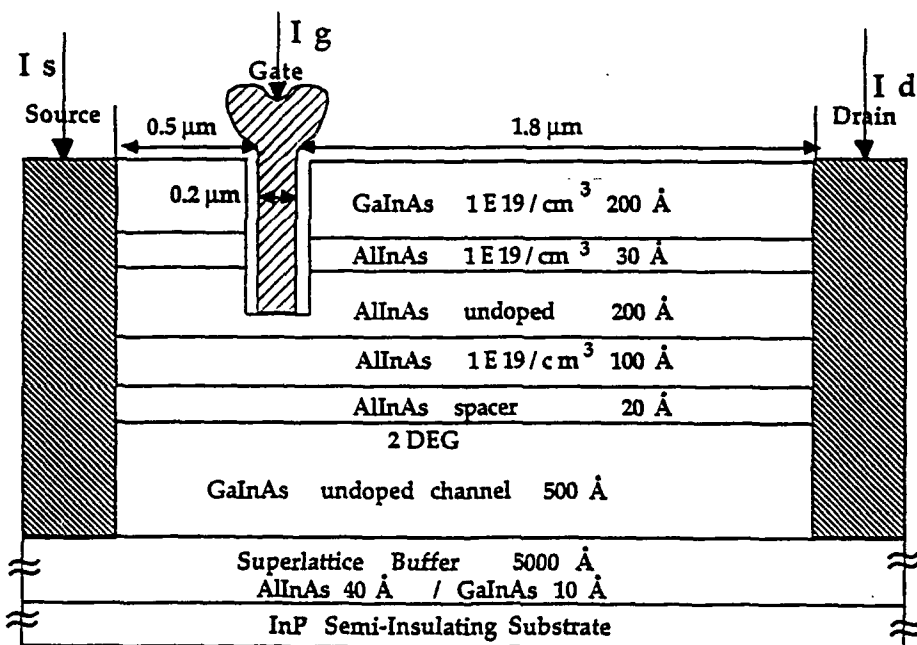
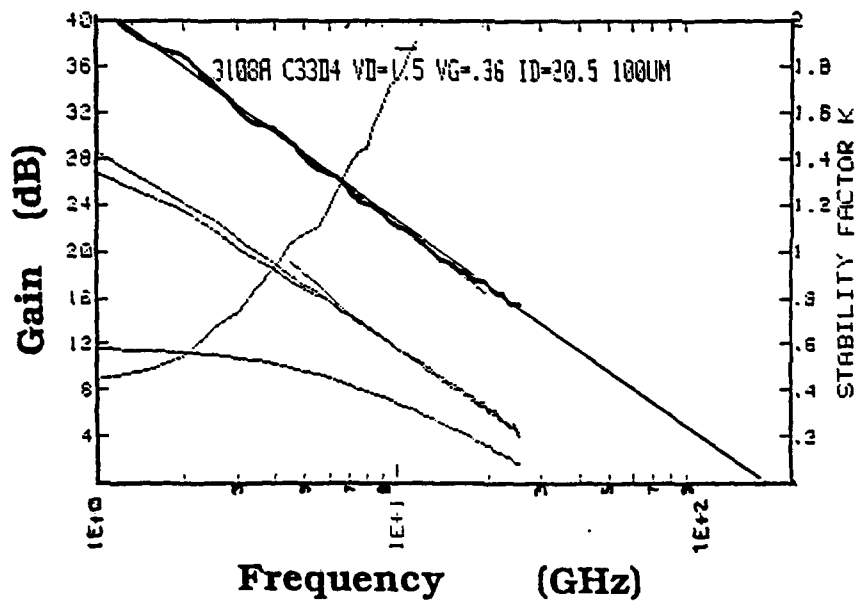


FIGURE 4



Cross-sectional View of 0.2 μm Gate Length AlInAs/GaInAs/InP MODFET

FIGURE 5



Current Gain Versus Frequency
 0.1 μm Gate Length AlInAs/GaInAs/InP
 MODFET
 AlInAs grown with low Arsenic over-pressure
 $f_T=140\text{-}150\text{ GHz}$
 $V_d=1.5\text{V}$, $V_g=+0.36\text{V}$, $I_d=205\text{mA/mm}$
 $R_s=1.4\Omega\text{-mm}$, 100 μm gate width

Figure 6

COMPOUND SEMICONDUCTOR STATE OF THE ART
2Q 1989 ON GaAs SUBSTRATES

MESFET

.1 μm M gate with AlGaAs buffer
600-700 mS/mm $f_{\text{tx}} = 115$ GHz
.25 μm gate with P GaAs buffer
Logic gate switching < 10 ps

MODFET

Doped $\text{Al}_{.3}\text{Ga}_{.7}\text{As}/\text{GaAs}$
.1 μm M gate, $g_m - 450$ mS/mm
 $f_{\text{tx}} = 113$ GHz
.25 μm M gate 1.8 dB noise figure at 60 GHz
5°K noise temperature at 8 GHz (12°K)
.25 μm logic gates switching < 6 ps at 77K

SMODFET

Doped $\text{Al}_{.3}\text{Ga}_{.7}\text{As}/\text{In}_y\text{Ga}_{1-y}\text{As}/\text{GaAs}$
.10 μm M gate, $y = .22$, $f_{\text{max}} = 345$ GHz, $f_{\text{tx}} = 60$ GHz
.14 μm M gate, $y = .25$, $f_{\text{tx}} = 153$ GHz
 $I_{\text{DS}} = 500$ mA/mm, $f_{\text{max}} = 250$ GHz
.25 μm M Gate, $y = .22$, 1W/mm, 50% power-added efficiency
.25 μm M gate, $y = .15$
1.6 dB noise figure at 60 GHz
20°K noise temperature at 8 GHz (12°K)

HBT

1.2 μm $5 \times 10^{17}/\text{cm}^3$ emitter, $1 \times 10^{20}/\text{cm}^3$ base
 $f_{\text{tx}} = 75$ GHz, $f_{\text{max}} = 175$ GHz
Logic switching time 14 ps
 $f_{\text{tx}} = 105$ GHz with ballistic electron collector

PBT

.25 μm period tungsten control electrodes in base
 $f_{\text{tx}} = 40$ GHz, $f_{\text{max}} = 265$ GHz

FIGURE 7

COMPOUND SEMICONDUCTOR STATE OF
THE ART
2Q 1989 ON InP SUBSTRATES

MISFET

1.0 μm gate with SiO_2 insulator
4.5 W/mm at 12 GHz, up to 45% efficiency

MODFET

Doped $\text{Al}_{.48}\text{In}_{.52}\text{As}/\text{Ga}_{.47}\text{In}_{.53}\text{As}/\text{Al}_{.48}\text{In}_{.52}\text{As}/\text{InP}$
.2 μm M gate - $g_m = 800 \text{ mS/mm}$
 $f_{tx} = 125 \text{ GHz}$, $f_{max} = 370 \text{ GHz}$
.8 dB noise figure at 60 GHz
Logic gate switching 6.0 PS @ 300 K, 4.8 Ps @ 77K
.15 μm M gate - $g_m = 1320 \text{ mS/mm}$, $f_{tx} = 186 \text{ GHz}$ (50 μm)

SMODFET

Doped $\text{Al}_{.48}\text{In}_{.52}\text{As}/\text{Ga}_{.35}\text{In}_{.65}\text{As}/\text{Ga}_{.47}\text{In}_{.53}\text{As}/\text{InP}$
.10 μm M gate, $f_{tx} = 210 \text{ GHz}$ (200 μm)

HBT

$\text{InP}/\text{In}_{.53}\text{Ga}_{.47}\text{As}/\text{InP}$ - 3.6 x 3.6 μm
Emitter doped to $.5 \cdot 10^{18}/\text{cm}^3$, base to $5 \cdot 10^{20}/\text{cm}^3$
 $f_{tx} = 165 \text{ GHz}$, $f_{max} = 100 \text{ GHz}$ @ 300K
 $f_{tx} = 244 \text{ GHz}$ at 77K

FIGURE 8

Ballistic Transport in the Plane.

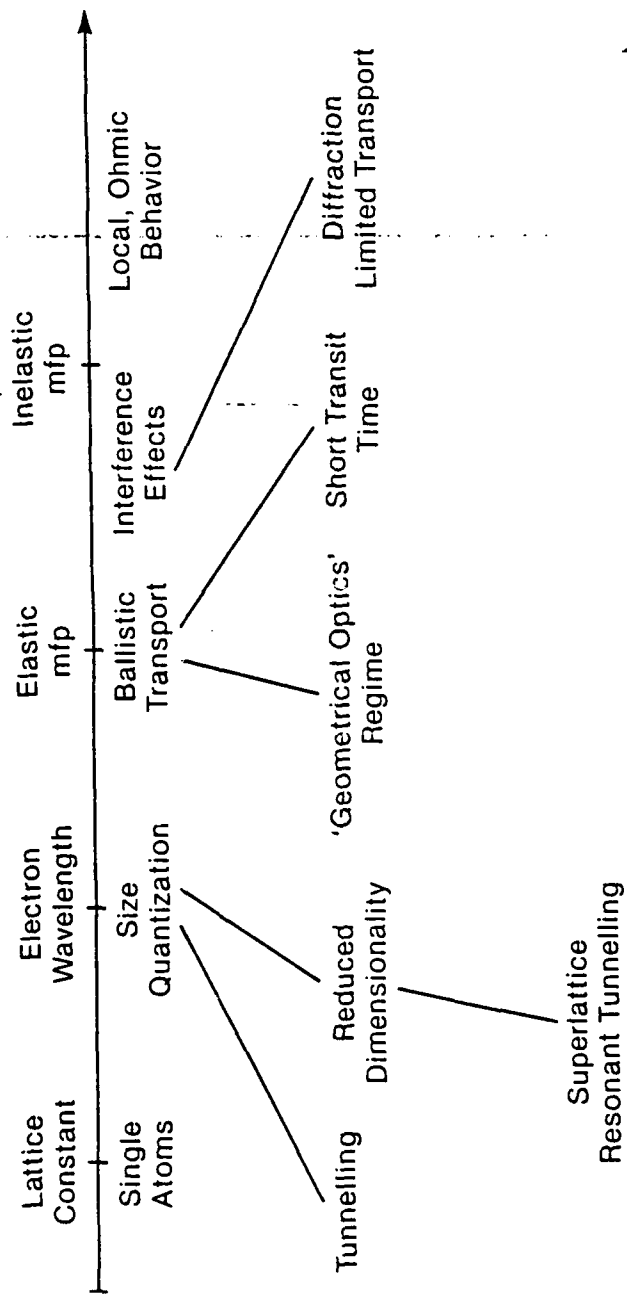
Invited : M. Heiblum, IBM Yorktown heights, USA.

BALLISTIC TRANSPORT IN THE PLANE

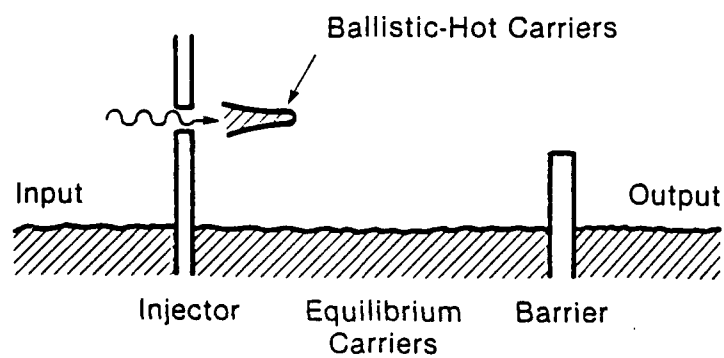
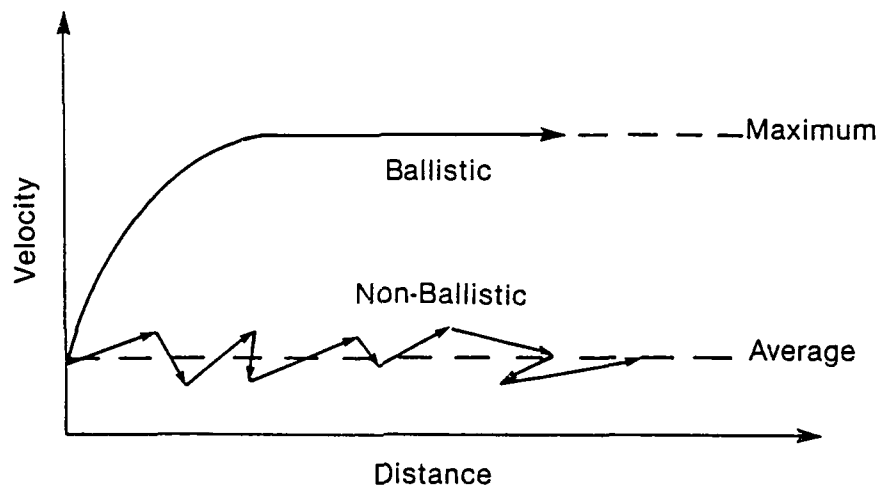
M. Heiblum, A. Palevski and C. Umbach

- **Ballistic Transport and Spectroscopy**
- **High Gain Ballistic Device**
- **Lateral Transport of Ballistic Electrons**

As Dimensions Shrink . . .

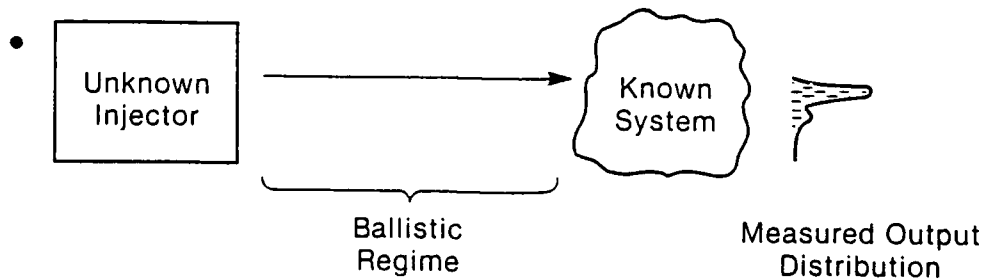
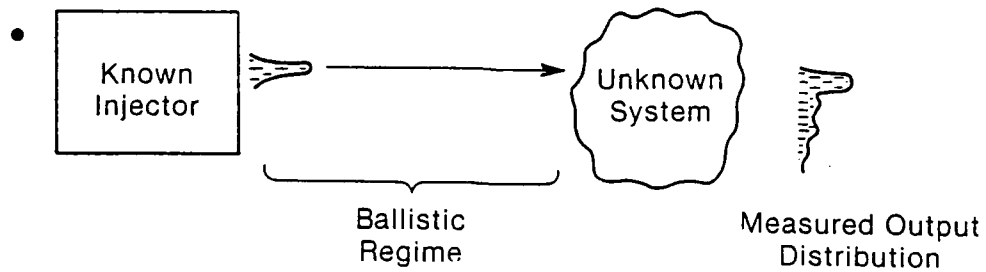
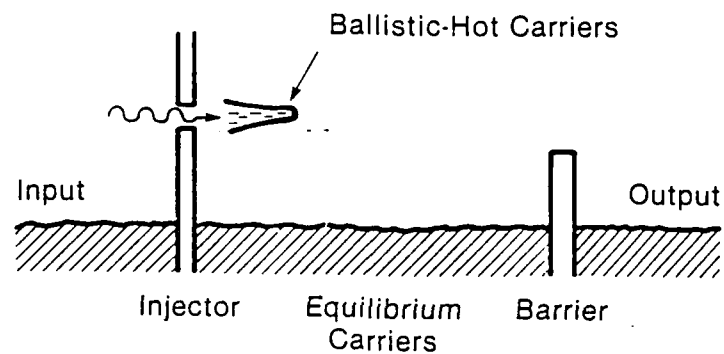


Why Ballistic?



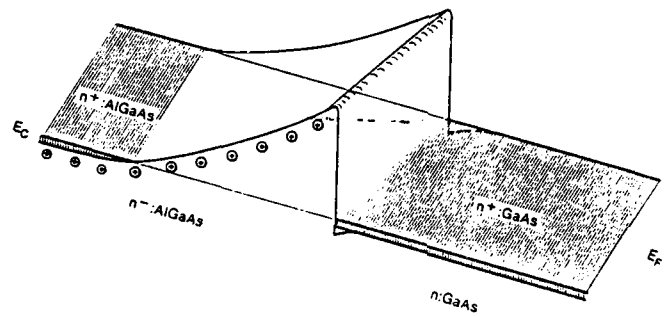
Employment of Ballistic Transport

- Device Applications: Fast Carriers

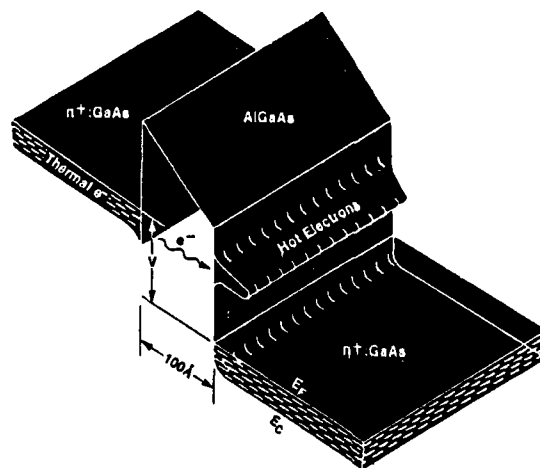


Injecting Hot Carriers

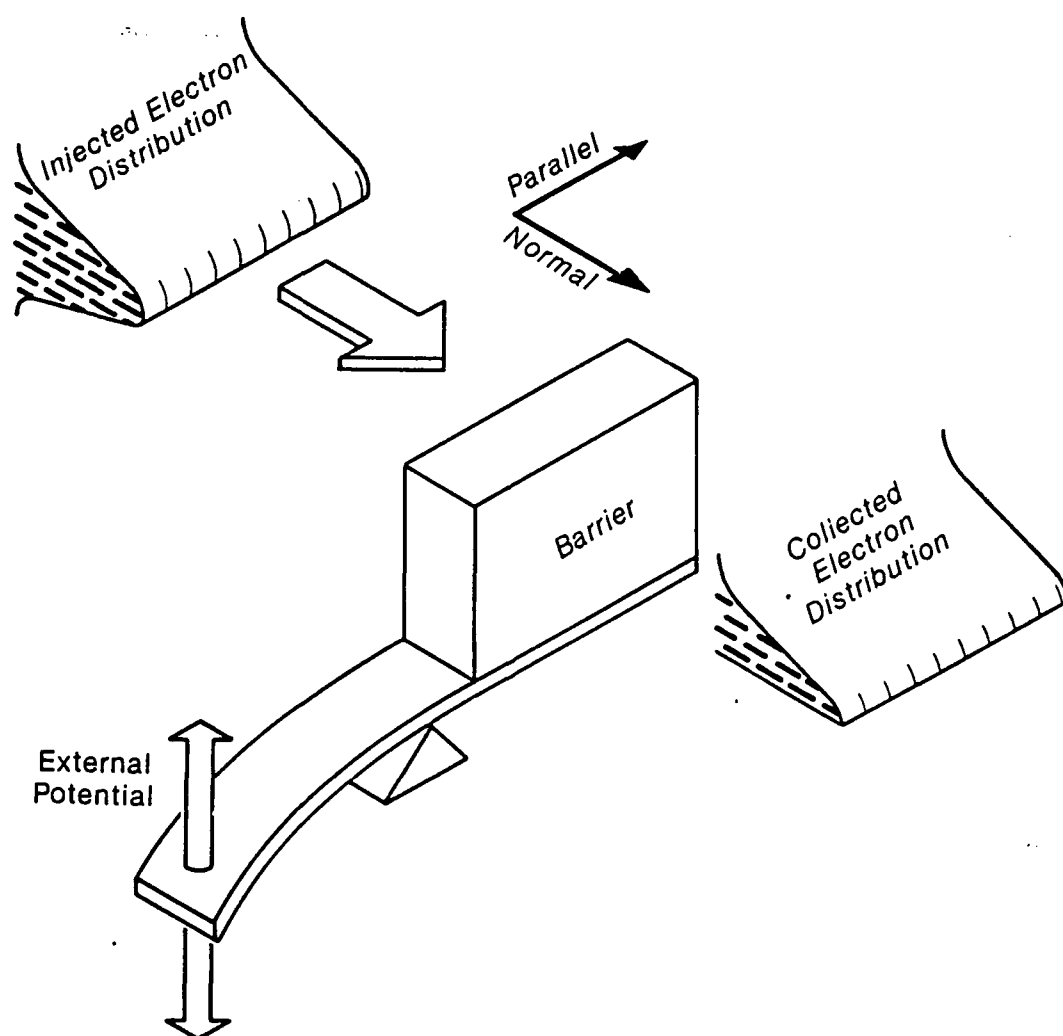
Thermal Emitter



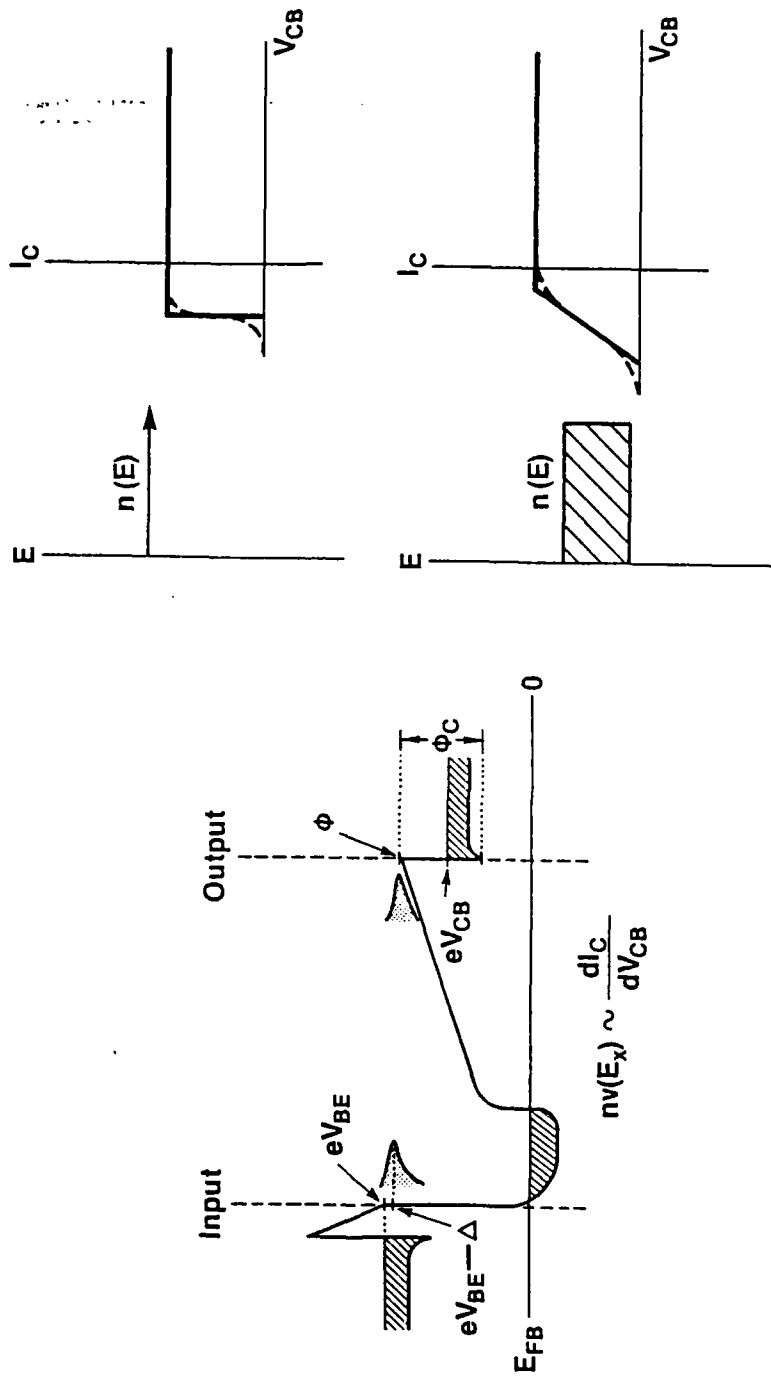
Tunnelling Emitter

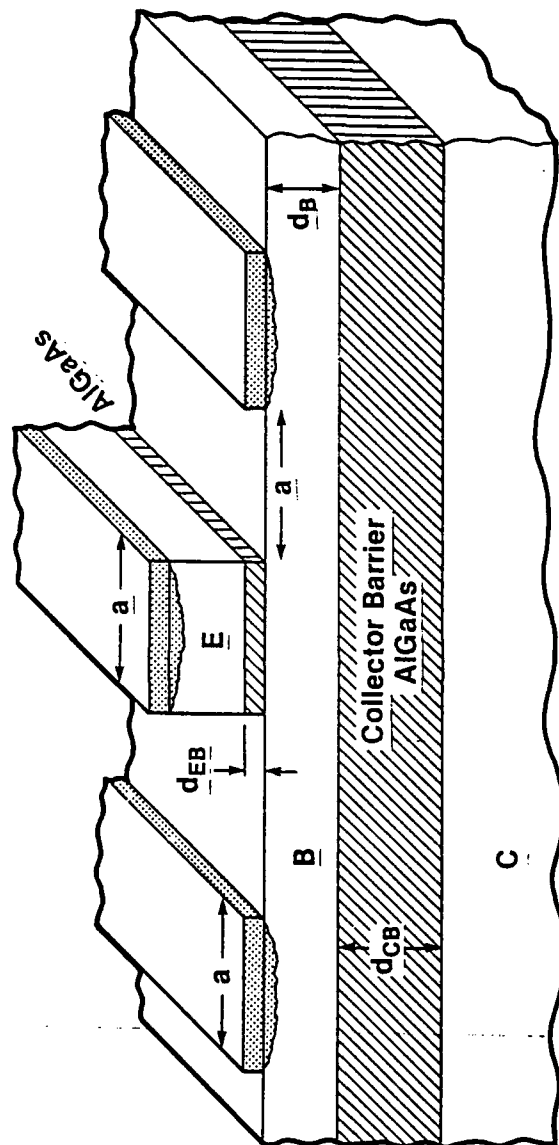


Doing Energy Spectroscopy



Energy Spectroscopy in a THETA Device

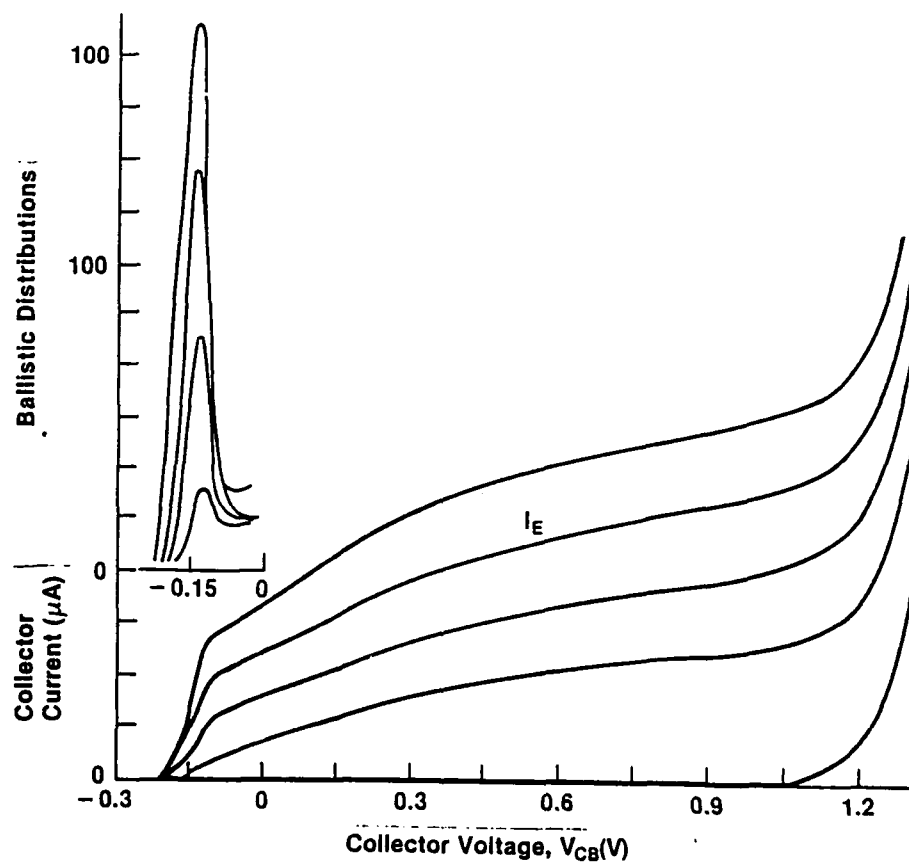




Typical Output Characteristics

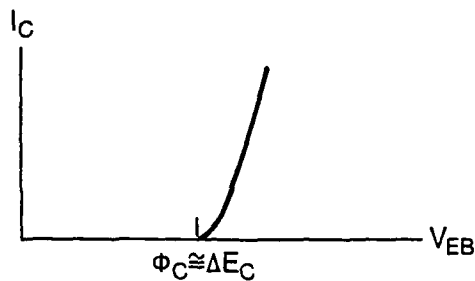
Base $\sim 30\text{nm}$

$n \sim 1 \times 10^{18}\text{cm}^{-3}$



Device Potential and Characteristics

- No Minority Carriers Storage Effects
- Current Gain Today ~ 30 at 77K
- Threshold Determined by AIAs Mole-Fraction



- For $J \cong 10^5 \text{ A/cm}^2$
 $0.25 \mu\text{m}$ Geometry
 $\Delta V = 0.1\text{V}$ } $\Delta t < 1\text{ps}$
- Problems:
 - Low Current Density
 - High Contact and Base Resistances

Device Achievements

- Until Recently : $\beta_{\max} \cong 9$
 - ↓
- Reduced Base Doping $\rightarrow 4 \times 10^{17} \text{cm}^{-3}$
 - $d_B \cong 250 \text{\AA}$
 - ↓
 - $\beta_{\max} \cong 13 \text{ (4.2K)}$
- Increase Γ -L Valleys Separation by an InGaAs Pseudomorphic Base
 - $\beta_{\max} \cong 40 \text{ (4.2K)}$
 - $\beta_{\max} \cong 30 \text{ (77K)}$

WHY LATERAL BALLISTIC TRANSPORT ?

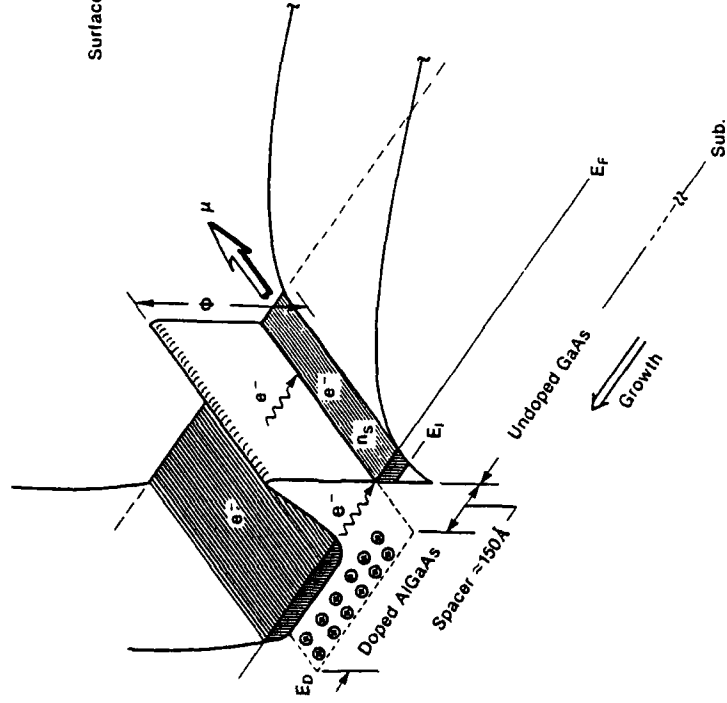
1. BEAM STEERING

- Ballistic Electrons Maintain Their Phase Coherence Over Length Scales on the Order of the Mean Free Path
- Their Behavior is Similar to Light Waves: They can Interfere, Reflect, Refract, etc.
- By Changing Their Velocity in Certain Regions the Effective Index of Refraction can be Modulated
- We Can Envision a New Field of Research: Electron Beam Steering in the Plane

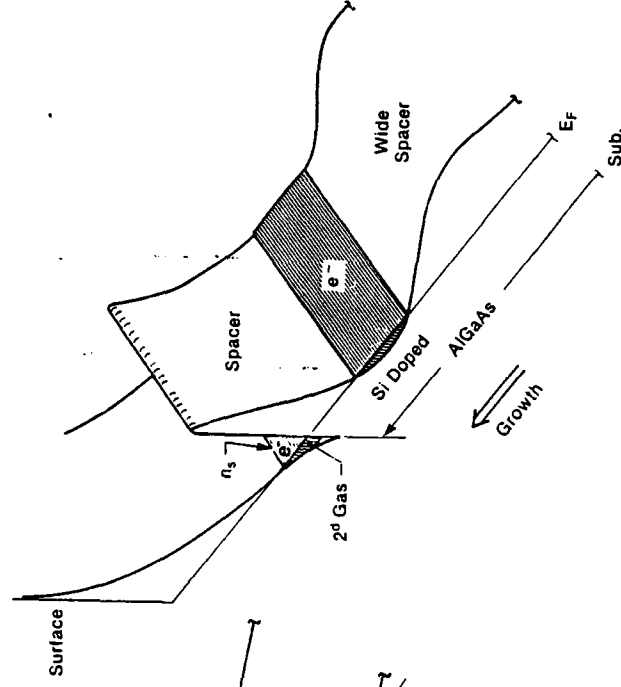
2. LATERAL HOT ELECTRON DEVICE

- Long Mean Free Paths are Achievable
- Easier Fabrication and Possible Integrability with FET type Devices

"Normal" Interface

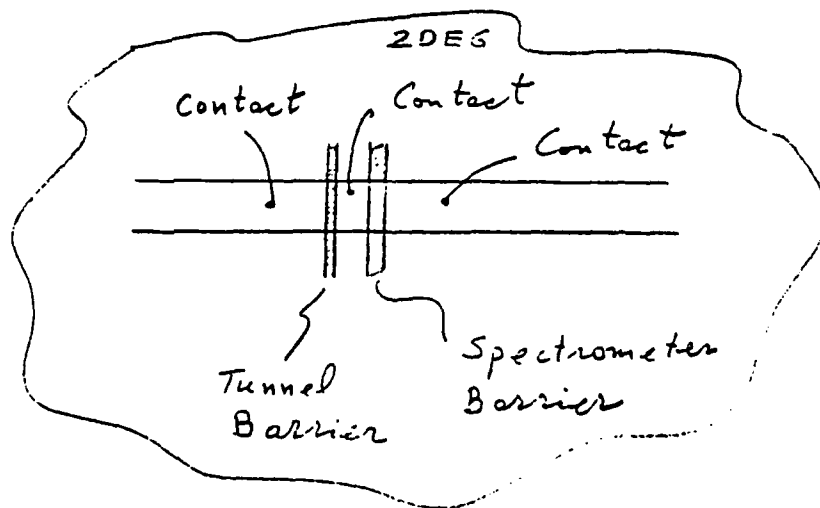


"Inverted" Interface

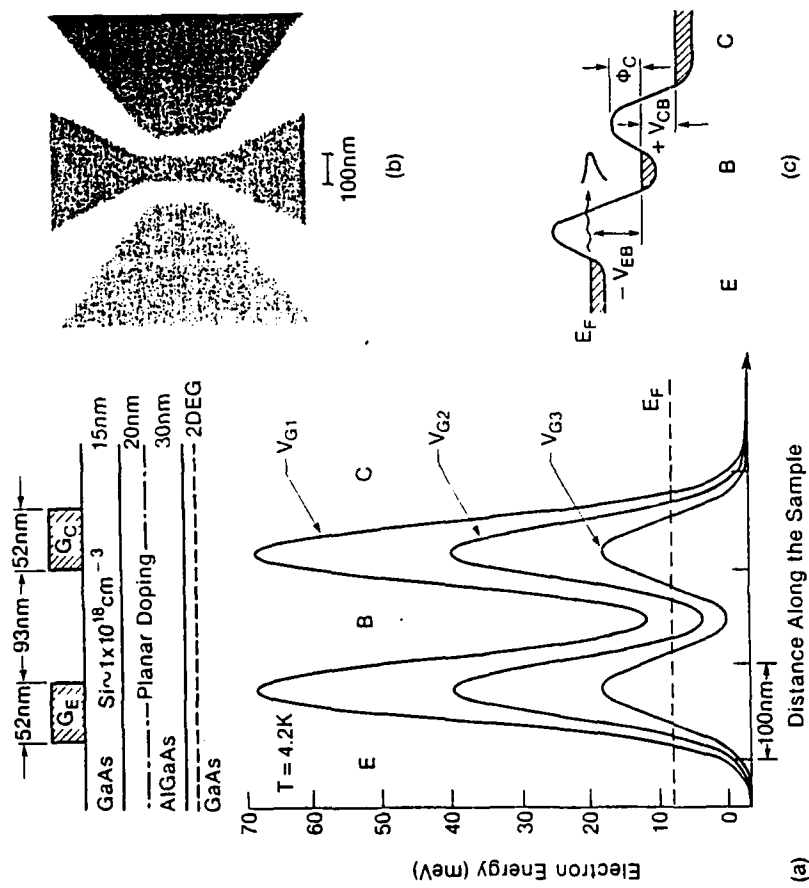


BALLISTIC TRANSPORT IN THE PLANE

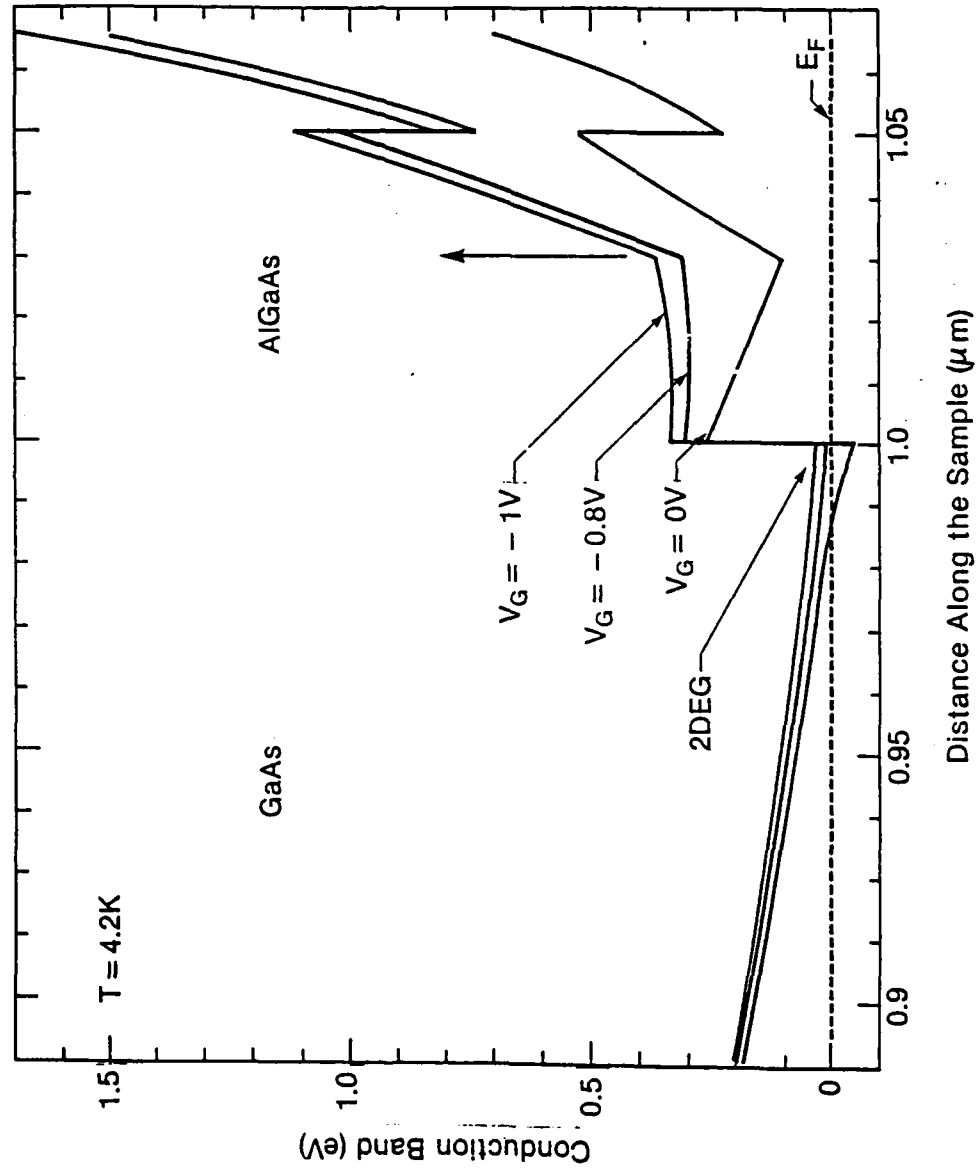
- Injection and Electron Spectroscopy in a 2DEG
- Building Barriers for Tunnelling Injection and Spectroscopy



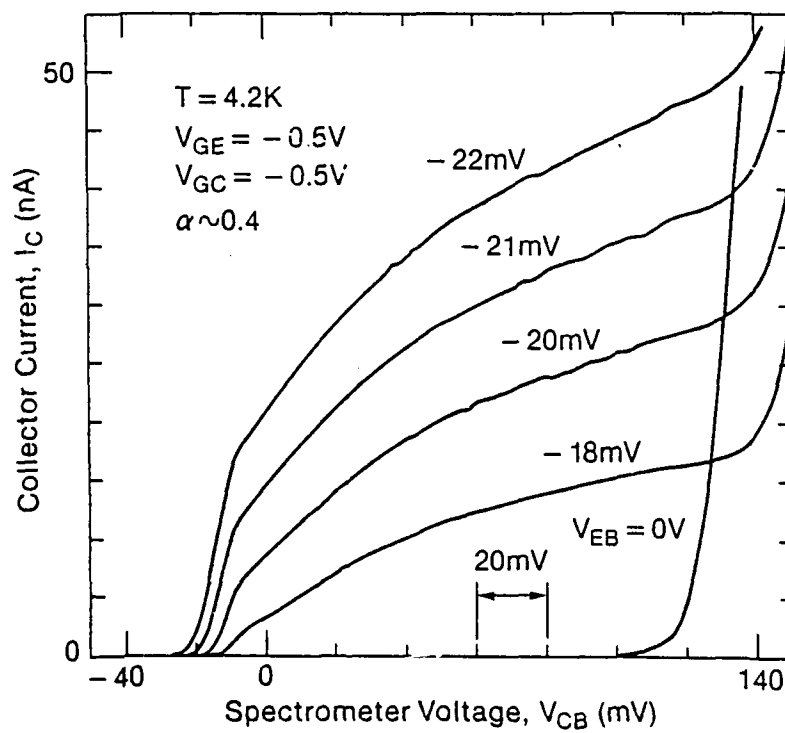
A Lateral THETA Device



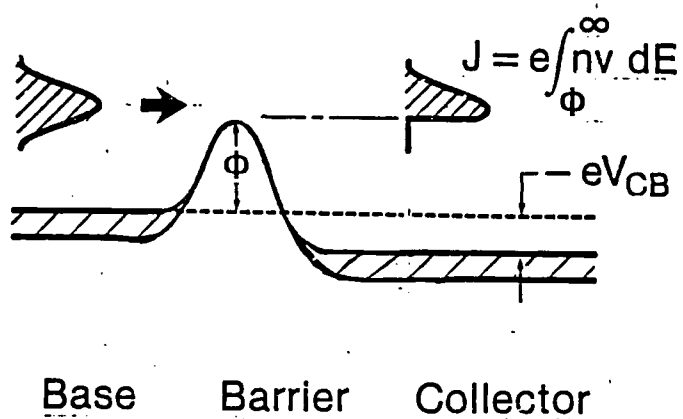
Biasing a 2DEG with a Gate



Output Characteristics in a Common Base Configuration



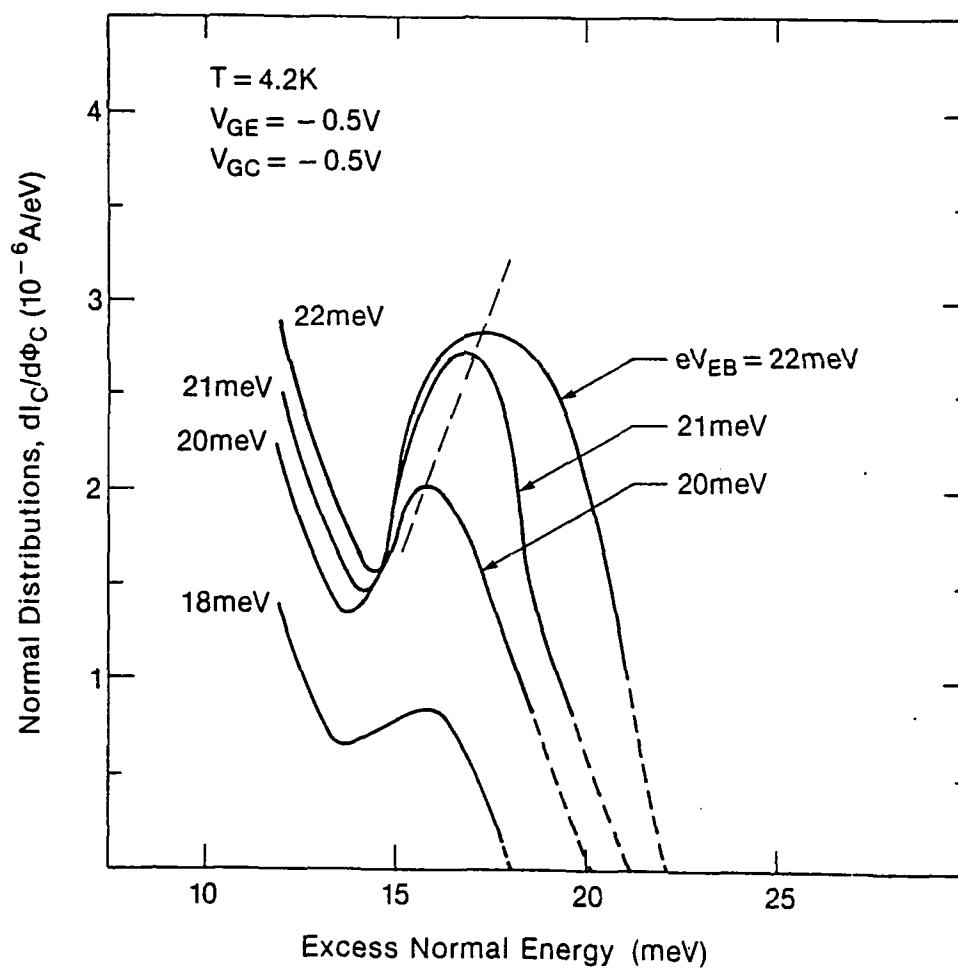
Spectroscopy of Ballistic Electrons



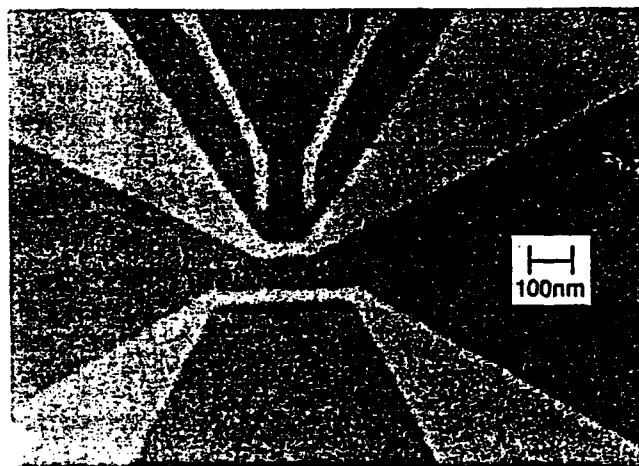
$$nv \sim \frac{dJ}{d\phi} = \frac{\frac{dJ}{dV_{CB}}}{\frac{d\phi}{dV_{CB}}}$$

Measured

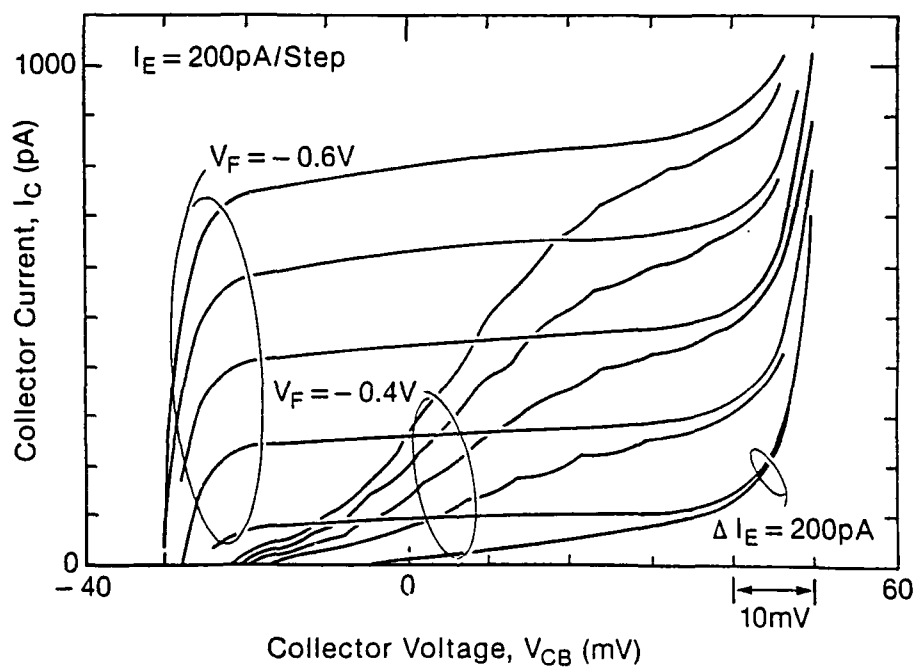
Lateral Ballistic Distributions



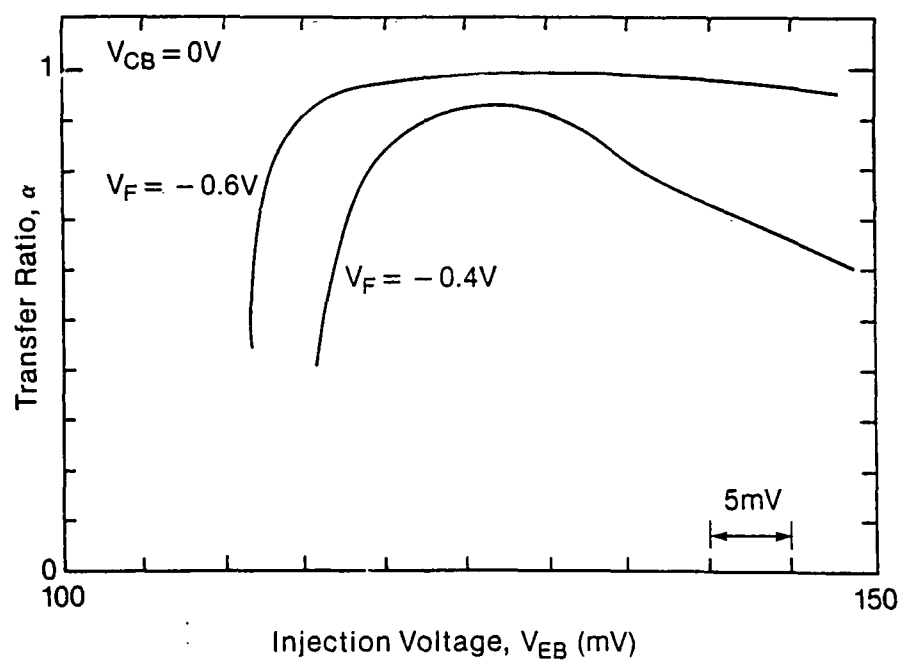
Side Gating



The Effect of Side Tunnelling



The Effect of Side Tunnelling

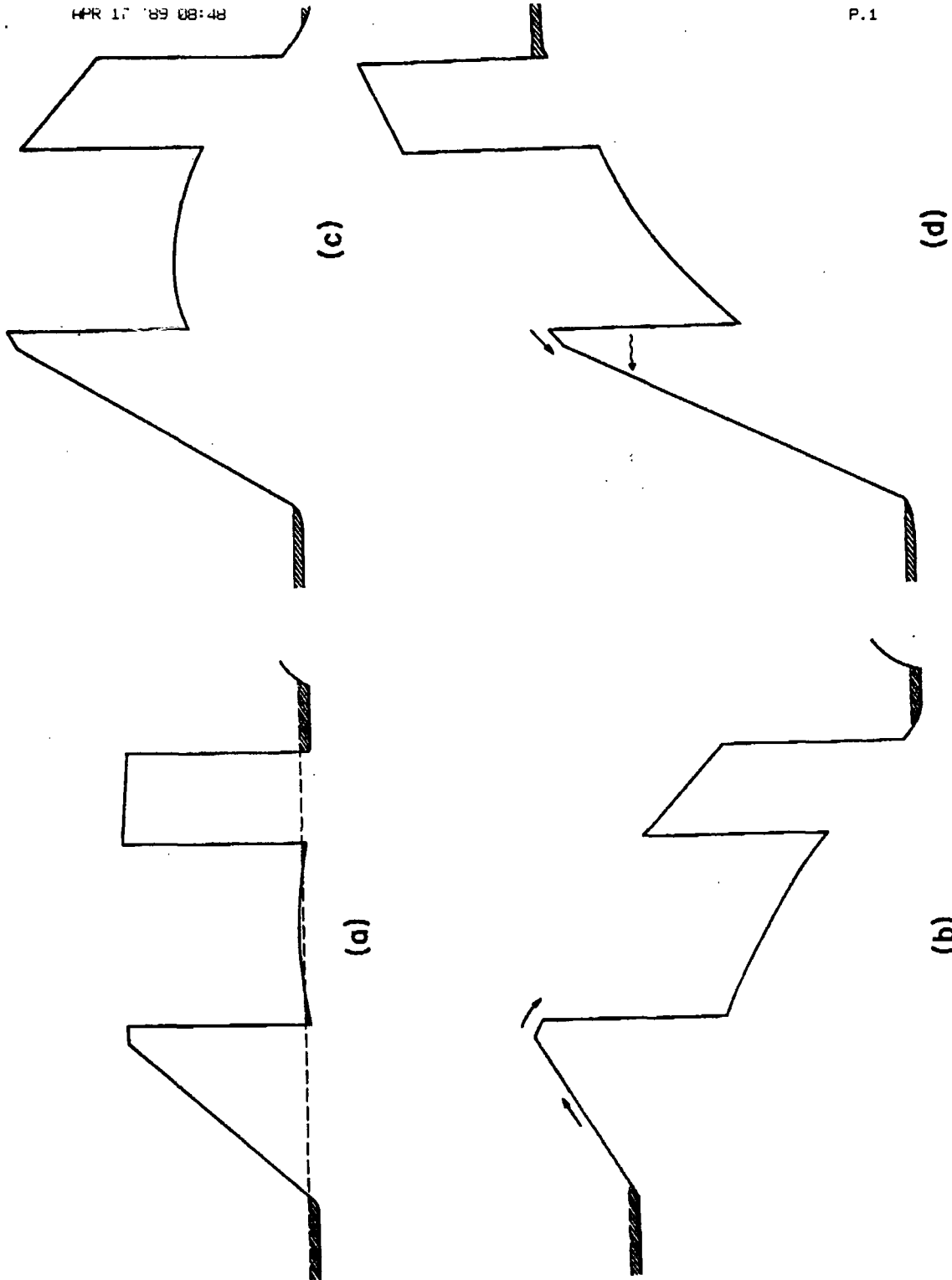


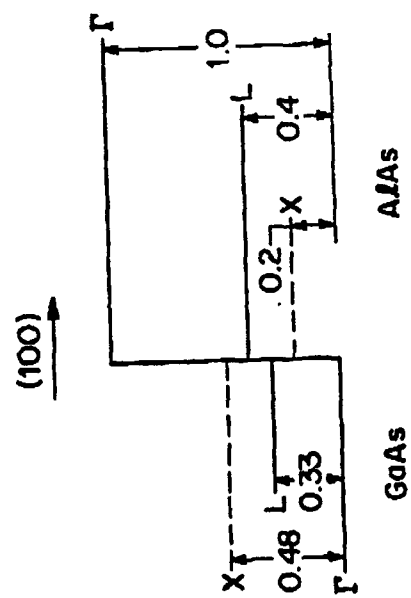
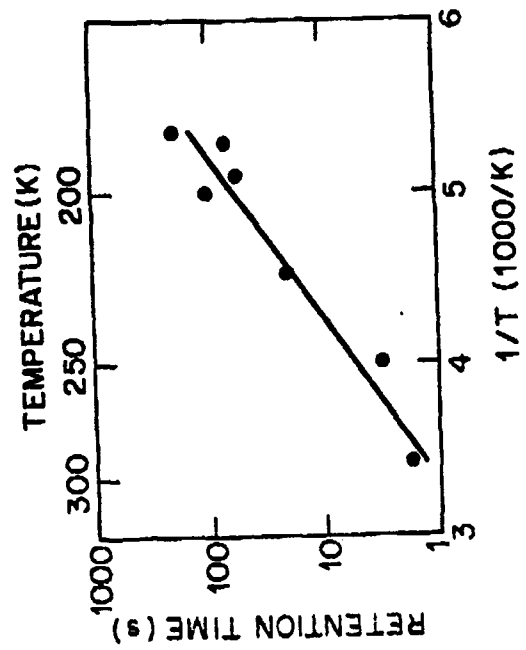
**Resonant Tunneling Transistors and New III-V Memory Devices for New
Circuit Architectures with Reduced Complexity.**

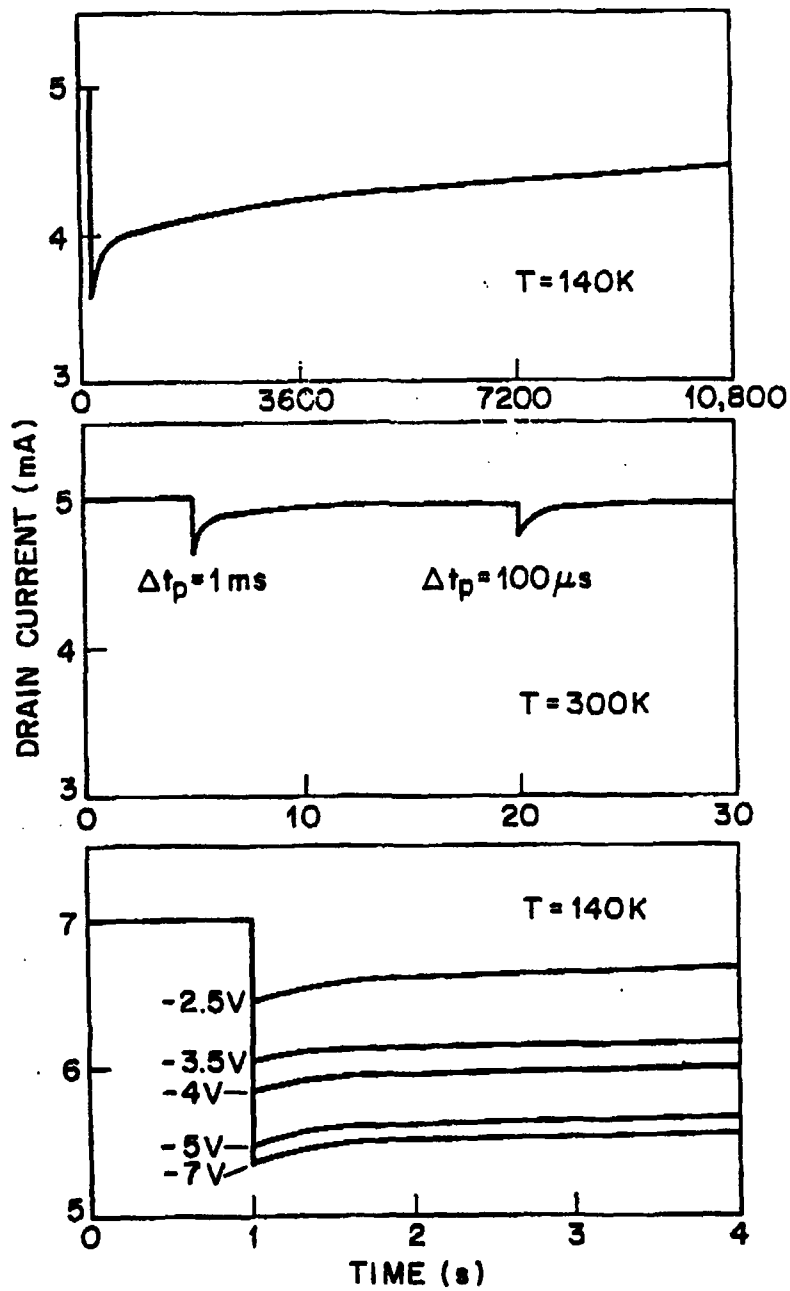
Invited : F. Capasso, Bell. Laboratories, Murray Hill, USA.

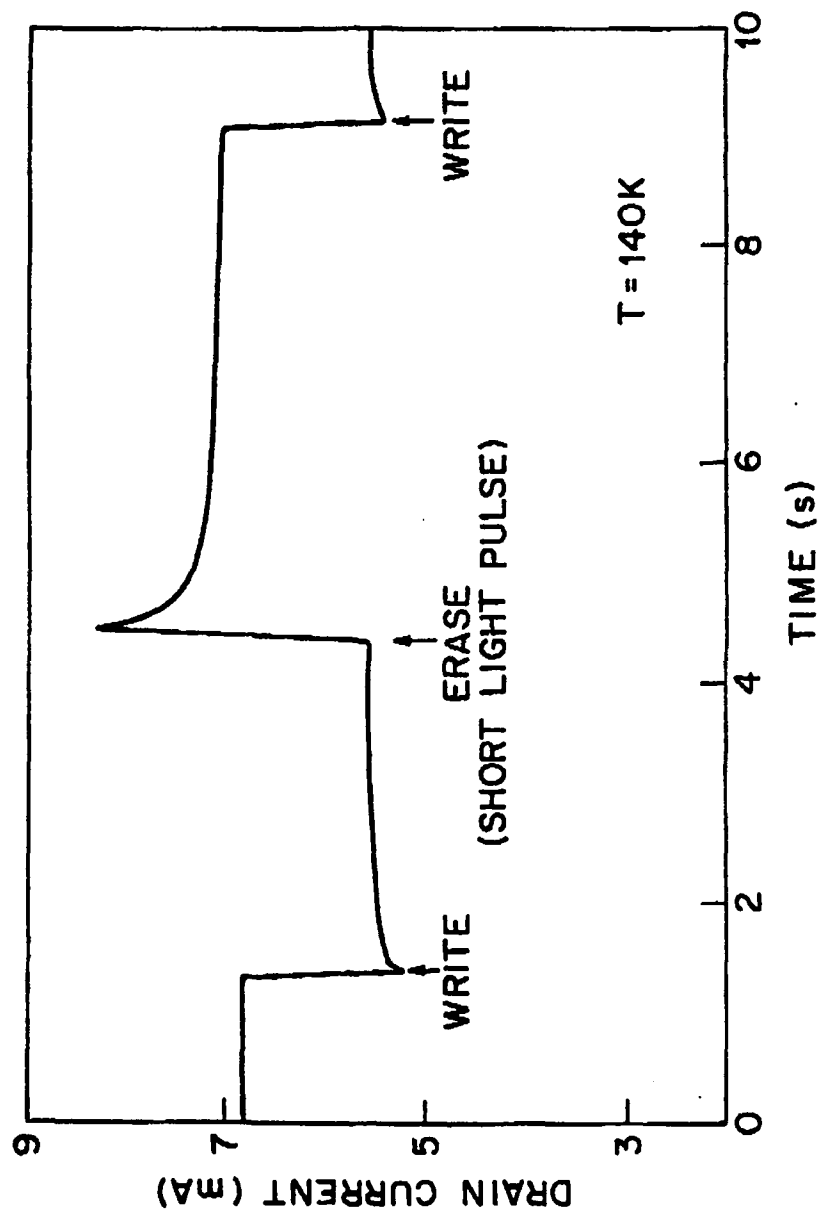
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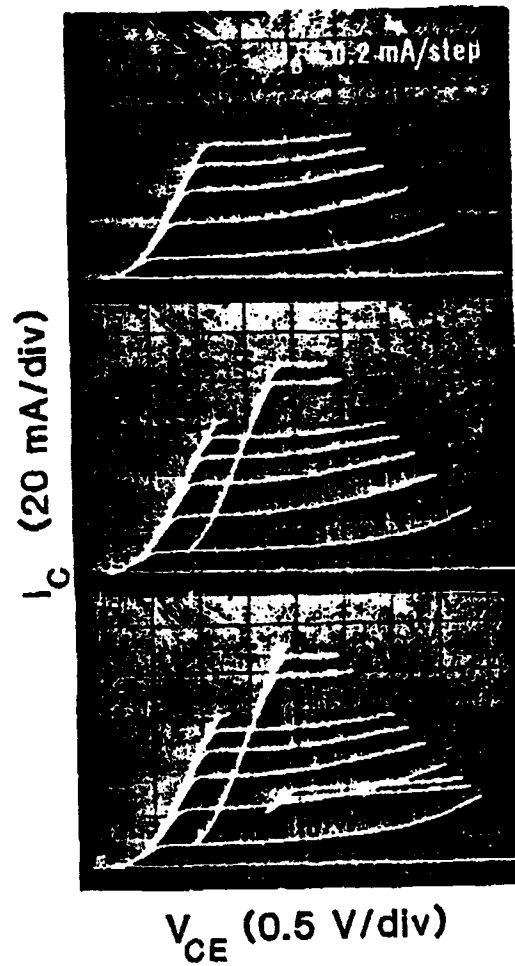
P.1

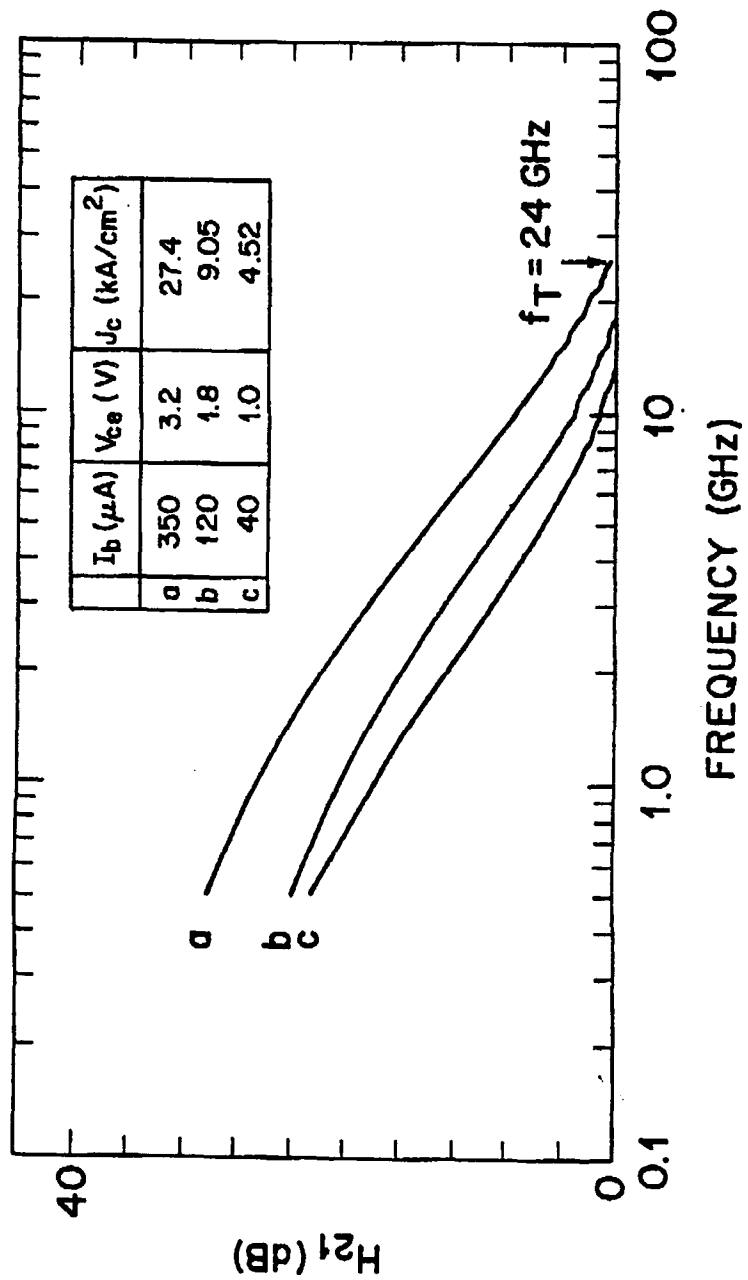


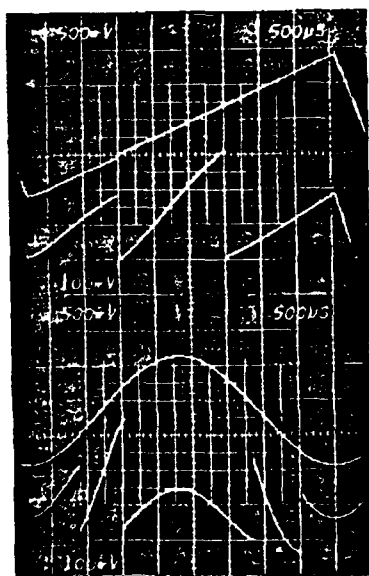
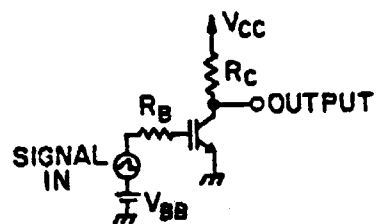


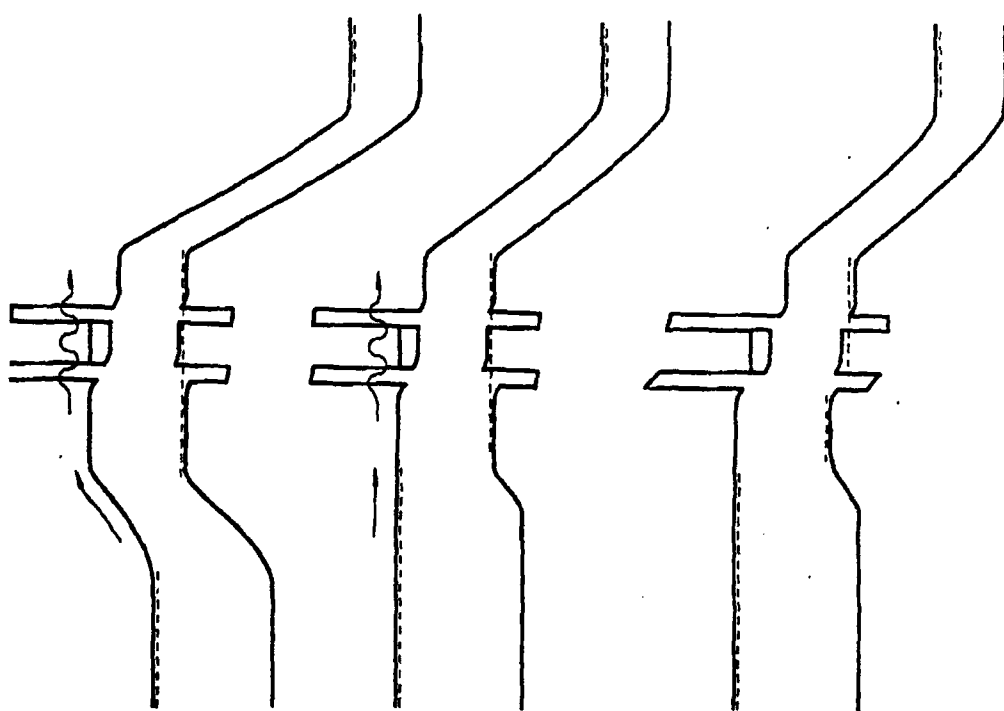




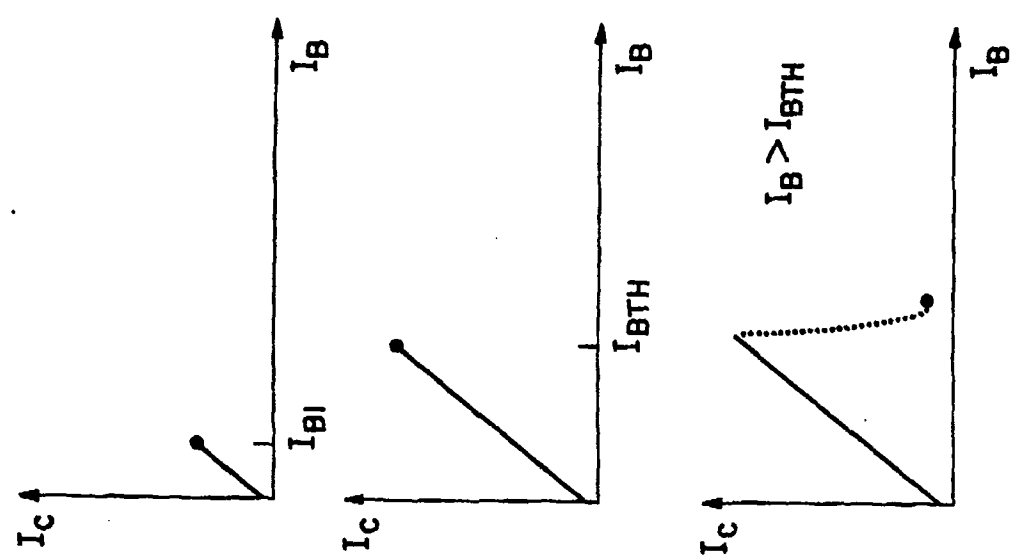








$V_{CE} = \text{const.}$



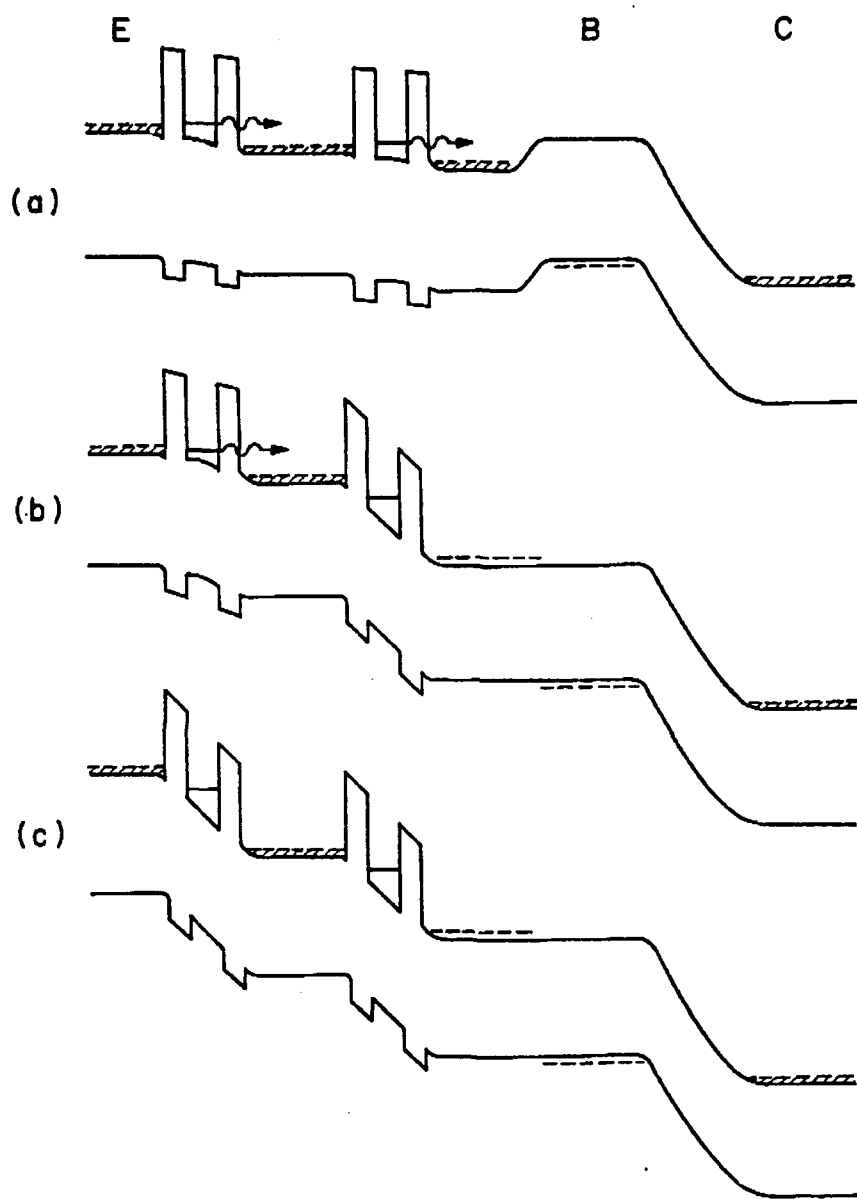
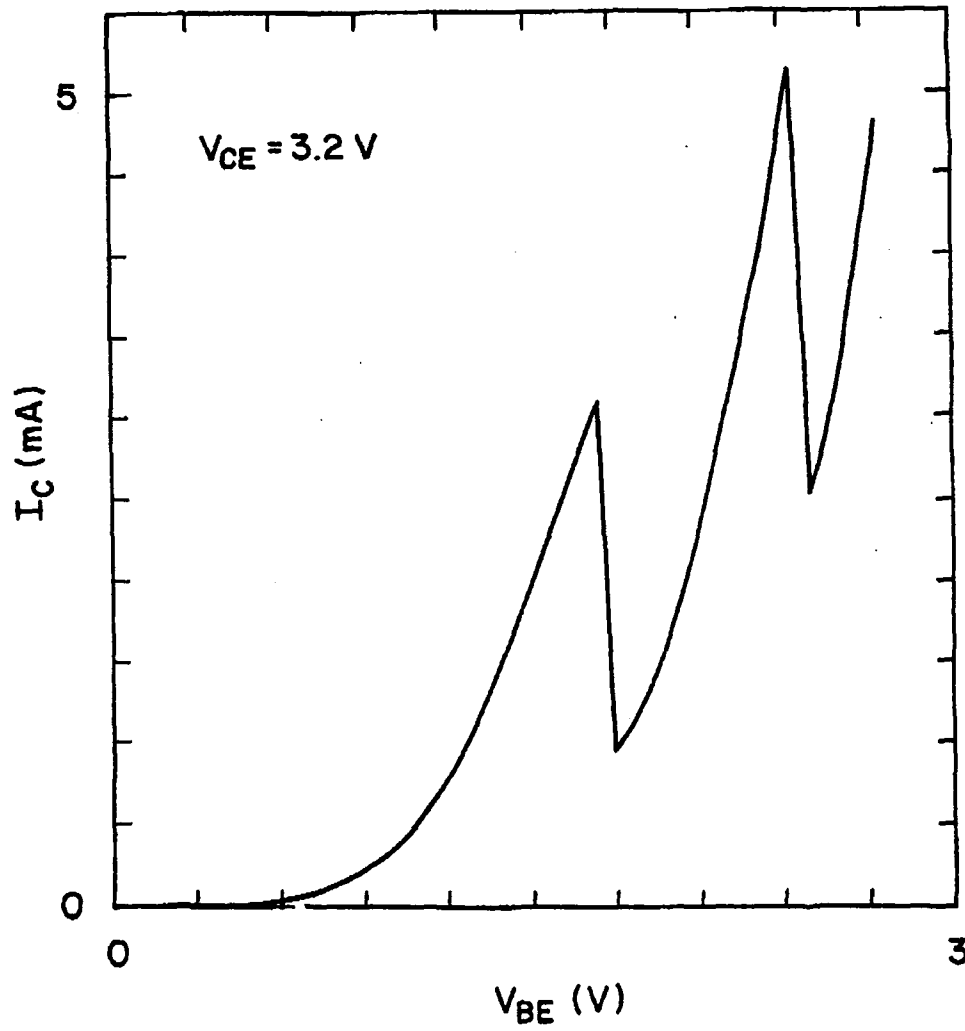


Fig 1.

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Millimeter-Wave GaAs ICs

Invited : W. Menzel, AEG Ulm, FRG.

Millimeter-Wave GaAs ICs

W. Menzel, B. Adelseck*

Abstract

A survey of GaAs monolithic integrated circuits is given with emphasis on the last 3 or 4 years. Primarily, Schottky diodes and MESFETs were the most often used devices, but in the meantime, HEMTs are playing an increasing role. First results have been achieved with HBTs, especially for power applications. For completeness, work based on Gunn elements and GaAs Impatts is reported as well. The range of realized components includes mixers, amplifiers, oscillators, switches, phase shifters, and components with more than one function.

Introduction

A low-cost, high-volume production of mm-wave equipment has to rely on the availability of monolithic integrated mm-wave circuits. Therefore, great efforts are undertaken to push the frequency limits of the necessary elements to higher frequencies, to provide suitable CAD tools and to design different circuit functions in a monolithic way /1/-/3/, /46/.

This contribution will mainly concentrate on the work done within the last years; however, the number of publications is so high and the progress in this area so fast that it will by far not be complete.

Most of the ICs are based on microstrip transmission lines as this type of line is best known to the designers, and a lot of design tools and CAD packages are available. Coplanar lines show advantages like series and shunt type connections on one substrate side without the necessity for substrate thinning /4/, /47/; design tools, on the other hand, are available only to a very limited extent.

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D-7900 Ulm, FRG.

Mixers

Mixer designs have been made as the first MMIC components in the mm-wave range. They are based on slot/coplanar junctions for crossbar type mixer arrangements /4/, on single ended configurations /5/, on rat-race couplers /6/, /8/, /23/, on Lange couplers /7/, /22/, and on hybrid ring couplers /21/, /42/-/45/. Worth mentioning is a subharmonically pumped mixer using two antiparallel Schottky diodes. The Schottky diodes itself show series resistances down to a few ohms, junction capacitances of a few fF and cut-off frequencies up to nearly 2000 GHz /44/.

As an example, a single sideband mixer based on two balanced mixers with hybrid ring couplers and an active IF hybrid is shown in Fig. 1. This mixer is part of an integrated 30 GHz satellite transponder /21/. Further efforts to combine mixer MMICs with RF preamplifier, IF amplifier or local oscillator chips for a complete receiver are reported in /20/-/23/. An integration of Schottky diode mixers together with transistor circuits on one chip /43/-/46/ gives special challenges for the technology; therefore such circuits are dealt with in a later chapter.

Low noise amplifiers

Compared to receivers with a diode mixer as first stage, an improvement in sensitivity is achieved using low noise preamplifiers. These are based on MESFETs /10/, /11/. /20/-/22/, /26/ as well as on HEMTs /13/, /14/, /16/-/19/. Compared to standard HEMTs, pseudomorphic HEMTs promise a further improvement in operation frequency and noise figure. Best results, however, have been achieved with InGaAs/AlInAs on InP /15/, giving 0.8 dB of noise figure at 63 GHz with an associated gain of 8.7 dB.

On GaAs substrate, best results are 1.2 dB and 1.8 dB noise figure at 32 and 60 GHz, respectively, for the transistors and 1.7 dB and 3.2 dB noise figure at 32 and 60 GHz with associated gains of 24 and 20 dB for a two stage amplifier /16/. 9.2 dB of maximum available gain at 92 GHz have already been achieved with 80 nm gate length HEMTs, and a transistor noise figure of 2 dB at 94 GHz is predicted /50/.

Based on HEMTs, extremely broadband amplifiers have been realized as well /17/-/19/ with bandwidths of 3-40 GHz, 2-43 GHz and 20-40 GHz, respectively. Gain is in the range of 6-8 dB, and minimum noise figures range from 3 to 4.2 dB. Fig. 2 shows a photograph and gain versus frequency of the 3-40 GHz travelling wave amplifier made by Varian /17/.

Power amplifiers and oscillators

Up to now, most mm-wave solid state transmitters rely on a direct modulation (AM, 2PSK) or on a complicated arrangement of upconverters followed by reflection type amplifiers (Gunn, IMPATT) or injection locked oscillators. A great improvement is achieved using three terminal devices, integrated in a monolithic circuit. Most amplifiers rely on MESFETs /24/-/29/, however HEMTs and HBTs show promising results as well /30/, /48/, /49/.

In the 30-35 GHz range, MESFET amplifiers achieve up to 1 W of output power with a gain of 4-5 dB as single stage amplifiers /28/, /29/. In the 50-60 GHz frequency range, typical output powers are in the range of 100 mW with 4-5 dB of gain /25/, /26/, /49/, and a balanced amplifier delivers 136 mW in the 56-61 GHz range /26/.

Broadband operation from 14-37 GHz with an output power of 100 mW is reported in /27/, while a MESFET VCO at 35 GHz is presented in /32/.

As an example for a power amplifier, a photograph of a 95 mW/55 GHz power amplifier designed by COMSAT /25/ is given in Fig. 3.

Gunn and IMPATT oscillators

Gunn elements and IMPATT diodes are widely used as discrete devices in mm-wave oscillators. Only within the last years, efforts have been made for their monolithic integration /31/-/35/. With Gunn oscillators, up to 125 mW in Ka-Band have been achieved /32/, while in V-band, this reduces to the mW range /31/.

Higher power levels are available from monolithic IMPATT oscillator, e.g. 100 mW at 61,5 GHz /34/. VCOs have been designed adding varactor diodes to the circuit. The varactor diodes have been derived from the IMPATT structures /34/, /35/.

Switches and phase shifters

For modulators, T/R switches and future mm-wave phased arrays, attenuators, switches, and phase shifters are of great importance. As semiconductor devices, PIN-diodes /36/, MESFETs /37/-/40/, varactors /40/, and Schottky diodes /41/ were employed. The PIN-diode switch operates in the 80-86 GHz range with an insertion loss of 0.5 dB and an isolation of more than 11 dB /36/. With MESFETs, extremely broadband operation can be achieved with 2-25 dB attenuation from 20-40 GHz and 3-23 dB from DC to 40 GHz /37/. In V-band, a 1.5 to 25 dB dynamic range is reported at 59-61 GHz with switching speeds below 1 ns.

In /39/, a bidirectional 3 bit MESFET phase shifter in the frequency range from 18 to 40 GHz with an insertion loss around 7 to 9 dB is described (s. Fig.4). At V-band, FETs and varactors are used for digital and analogue phase shift, respectively, using branch line couplers /40/. Instead of the FETs and varactors, Schottky diodes together with branch line hybrids are employed in /41/ for a 3 bit V-band phase shifter.

Integration of several functions on one chip

For a mass production of mm-wave systems, as it is expected for military (e.g. seekers) or traffic applications, a high degree of integration is desired. Especially, if different active elements have to be combined on a single chip, new ways have to be found for the technology to achieve optimum results. Two examples shall be given here. In /42/-/44/, Schottky diodes and MESFETs are integrated using a selective ion implantation for a buried layer to reduce the series resistance of the Schottky diodes. The active layer for the diodes as well as for the FETs is grown by MOCVD (Fig. 5).

In this way, diodes with cut-off frequencies up to 2000 GHz and MESFETs with f_{\max} 70 GHz have been realized. Fig. 6 show an integrated diode mixer and an IF amplifier on one chip /42/.

In /45/, HEMTs and Schottky diodes are combined. First, the HEMT layers are grown with MBE. A GaAlAs layer is used on top of this structure as an etch stop for reactive-ion-etching. On this layer, the diode layers are grown (Fig. 7). In this way, the diodes are realized as mesa type structures. HEMTs with f_{\max} 120 GHz and diodes with f_c 1250 GHz for W-Band operation have been realized in this way.

Conclusion

It has been shown - in a very condensed form - that a wide variety of GaAs MMIC activities exist. Performance is improving and operating frequencies are increasing nearly from month to month. Additionally, new active devices like hetero bipolar transistors, permeable base transistors, hot electron tunnelling structures, MISFETs and others are coming up, giving the chance to built high quality, sophisticated but modest to low cost mm-wave equipment.

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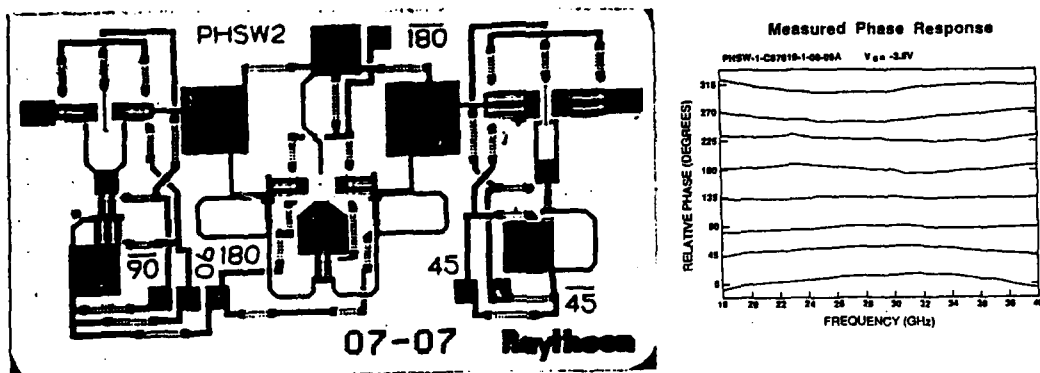


Fig. 4: K/Ka-band phase shifter, /39/

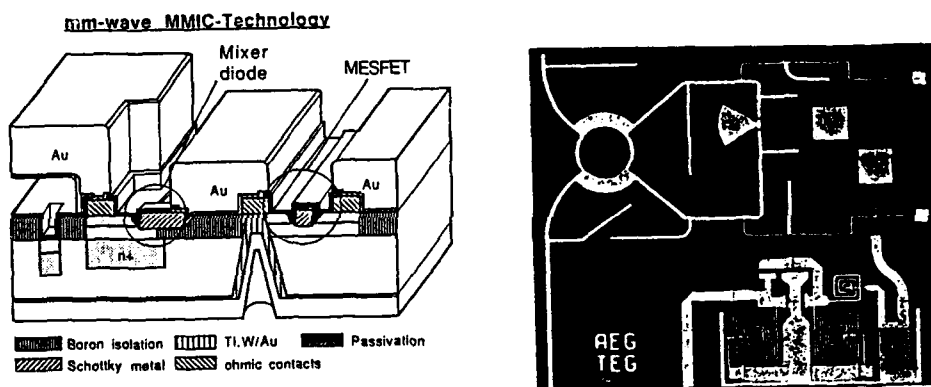


Fig. 5: Cross section of active devices for the combination of Schottky diodes and MESFETs, /42/-/44/

Fig. 6: 35 GHz integrated receiver chip, /42/.

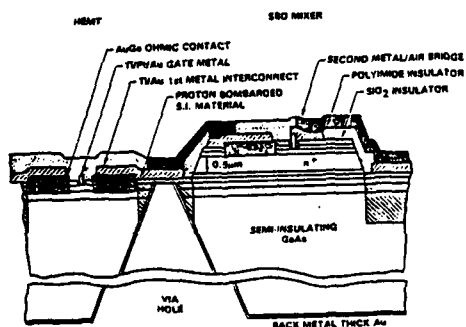


Fig. 7: Cross section of active devices for the combination of HEMTs and Schottky diodes, /45/

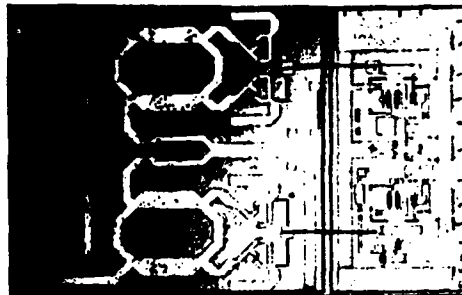


Fig. 1: Ka-band single sideband mixer, /21/

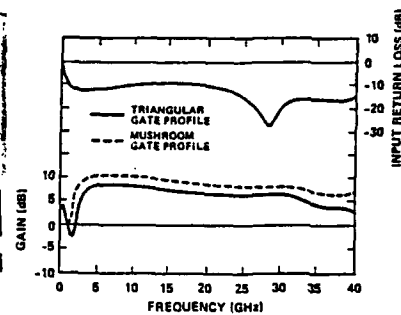
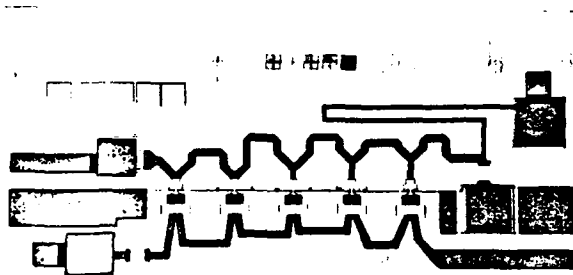


Fig. 2: Photograph and gain of a 3-40 GHz travelling wave amplifier, /17/

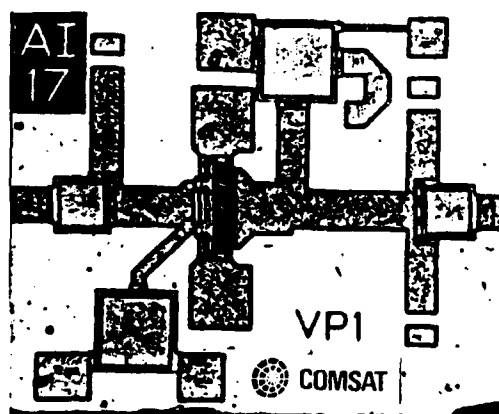


Fig. 3: V-Band power amplifier, /25/

TECHNOLOGY 1

LARGE AREA GROWTH OF OPTOELECTRONIC STRUCTURES IN THE LP-VPE SYSTEM

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Beside high rates of deposition (over 300 $\mu\text{m}/\text{h}$ for GaAs) the low pressure hydride VPE technique demonstrates unexpected capabilities for very large scale growth of III-V compounds. Taking advantage of the change in growth mechanism at pressures below 40 mbar deposition can be performed on substrates placed perpendicular to the direction of the main gas flow. This way the process becomes very similar to procedures which have been in successful use in the Si-technology for many years.

The growth behavior in the reactor was investigated at 10 mbar using 3 substrates separated by 5 mm. At the early stage of this study an thickness inhomogeneity on each substrate of around $\pm 9\%$ is obtained - without significant deviation of the thickness and the thickness profile from wafer to wafer. An improvement of this value is expected, when further reducing the overall reactor pressure. Using this approach the rate of deposition decreases by about a factor of 2 in comparison with that on substrates placed parallel to the gas flow. Furthermore, it appears that the electrical and optical properties of the films are the same, independent of position. This makes the LP-VPE system very attractive for the production of optoelectronic device structures.

EPITAXIAL GROWTH ON InP SUBSTRATES
ETCHED WITH METHANE REACTIVE ION ETCHING TECHNIQUE

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Fabrication of optoelectronic devices and their integration with microelectronics circuits require, in most cases, the growth of epitaxial layers on substrates which have been etched. Till now, wet chemical techniques are commonly used ; but recently plasma RIE based on methane, argon, hydrogen mixtures have been demonstrated to be efficient for etching GaAs, GaAlAs, InP, GaInAs, GaInAsP and GaSb. It seems likely that the reaction of CH_4 and H_2 in etching these III-V materials leads to the formation of volatile effluents such as metal organic compounds and hydrides (for example , $\text{In}(\text{CH}_3)_3$ and PH_3 , respectively for the case of InP). This technique permits good control of the etching depth and gives very smooth surface.

After etching, InP surface have been characterized by angle-resolved X-ray photoelectron spectroscopy ; this technique allows to determine the residual damage at the surface. Depending on the RF power (from 20 to 100 Watts) in the reactor and on the composition of the mixture, we found at the surface of InP a small layer which is depleted of phosphorus atoms. The thickness of this non-stoichiometric layer varies from 10 to 30 Å.

Using a gaz source MBE system, we have found that annealing under cracked PH_3 is able to restore the surface cristallinity. For example, after heating at 525°C during 5 mn, the residual damaged layer is reduced to about 1 monolayer. With this procedure, we obtain high quality InP epitaxial layers with doping level in the 10^{15}cm^{-3} range and mobilities values around $30000\text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ at 77°K for 1 μm thick layers. These results are similar to those obtained on chemically etched surfaces and demonstrates that RIE technique is suitable for devices fabrication.

InP plasma epitaxy

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The use of plasma excitation for a low temperature epitaxial process is a most promising technique with the aim to obtain sharp interfaces without destroying the layers produced. We have built up a system to grow epitaxial InP layers from solid sources (red phosphorous and metallic indium) by hydrogen plasma excitation. Such a process shows many advantages. The reactive atoms and ions and the increased migration on the bulk surface allow to decrease the growth temperature. In particular, the following two advantages can be quoted:

- In-situ cleaning by H_2 plasma removes the native oxides at low temperatures
- Using solid sources no toxic gases or organic compounds have to be stored or handled. There is also no need for a rather expensive UHV system.

We have grown epitaxial layers on semiinsulating $\langle 100 \rangle$ InP material (which was pretreated in HF) at temperatures of 350°C and 400°C . No significant differences between the epitaxial layer grown at 400°C and a reference sample could be seen by XPS analysis of the surface. In-depth XPS analyses indicate that, at a sample temperature of 400°C , we grew an epitaxial layer without detectable differences to the bulk material. At lower temperatures (350°C) we deposited a layer rich in phosphorous. This corresponds to van der Pauw measurements.

The layer grown at 400°C is n type as expected for undoped InP. Before we optimized the process we measured a carrier concentration of $n \approx 10^{19} \text{ cm}^{-3}$ and a mobility of $200 \text{ cm}^2/\text{Vsec}$. In contrast to this, layers deposited at 350°C are p type which is not yet fully understood.

MOVPE grown Heterostructures for Monolithic Integration

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The use of MOVPE as a tool for monolithic integration requires basic work on:

- 1.) semi-insulating layers
- 2.) selective area growth
- 3.) development of the InGaAlAs/InP-system

Using ferrocene as metalorganic source material we have grown semi-insulating InP layers with resistivities up to $\rho = 2 \cdot 10^9 \Omega \text{cm}$. The resistivity of the layers (iron content in the crystal) is a linear function of the iron content in the gas phase. With these layers crystal quality of undoped layers could be achieved.

Growth behavior on different geometries and reactor pressures was studied. By optimizing these parameters, selective area growth resulting in planar surfaces was possible.

InAlAs layers were grown with net carrier concentrations in the low 10^{16}cm^{-3} range and with mobilities up to $2600/6500 \text{ cm}^2/\text{Vs}$ at 300/77 K, respectively. Schottky barrier heights of 0.8 eV with an ideality factor of 1.08 were measured typically.

DEVICE 1

Two-Dimensional Simulation of the Electron Diffusion Field-Effect Transistor

by

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In this work, GaAs EDFET's (electron diffusion field-effect transistors) are analyzed by using a full dynamic transport model which consists of the particle conservation equation, the time-dependent momentum conservation equation, and the energy conservation equation as well as Poisson's equation. The calculations show:

- 1.) At the drain edge of the channel, there occurs a smaller static domain in the EDFET than in the normal FET, because of the excess electrons from the high-doped channel region.
- 2.) The gate capacitance decreases versus the width W_{L0} of the low-doped region.
- 3.) The transconductance of an EDFET is higher than that of a normal FET because of an additional current which is caused from the excess electrons. The transconductance of the EDFET increases with increasing width of the low-doped region until a maximum value at $W_{L0} \approx 0.2 \mu\text{m}$. For larger W_{L0} , it decreases.
- 4.) There is an optimum width of the low-doped region. The cutoff frequency of an EDFET with this optimum width is higher by about 20 % than for a normal FET.

Parameter Estimation Tool for GaAs MESFETs.

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A fully automated parameter estimation and model evaluation system is presented in this paper. Initially, the tool was designed for the GaAs MESFET, but it can be easily extended to include models for other passive or active devices, as the software is written very modular.

The model optimisation uses a stable and efficient non-linear least squares algorithm or a quasi-Newton algorithm for general function minimisation, which allows for large deviations between the initial estimations for the parameters and their final optimised value. This means that the initial estimations can be calculated automatically, without operator's interference.

The model, implemented in the system, is derived from the well-known Curtice-model [1]. The further developments, a modified topology and the expression proposed by Takada et al. [2] for the bias dependence of the gate-capacitance are also evaluated by means of this tool.

The implemented model is valid for low pinch-off voltage devices ($V_T > -2$ V). The extended topology already accounts for some of the effects that arise when V_T is lower, but to allow accurate simulation of these devices, some features need to be added to the DC current expression. Up to now, the model was only used in the simulation of digital circuits. In digital applications, mostly low pinch-off voltage devices are used. The model accuracy is certainly sufficient for these applications (model validity goes up to 18 GHz).

The system offers the possibility of determining all parameters for a complete GaAs MESFET transient model by optimizing the model responses. All available measurements are taken into account at the same time: drain current and gate current in DC, CV-measurements on the gate-junction and S-parameters in a common-source configuration at different bias conditions.

The implemented model has 23 different parameters (9 for the DC-model) to be determined. Even with this large number of unknown variables, interactive input is not necessary and the required CPU-time (on a VAX-station 3200) is typically less than the time needed to actually perform the measurements on an automated measurement set-up.

As mentioned above, it is not difficult to implement new models. An extended diode model (that includes the effect of distributed series resistance) and a DC-model for bipolar transistors are already provided.

In conclusion, we may state that a fully automated parameter estimation system for the GaAs MESFET was developed. This system can easily be extended for other devices and allows quasi on-line evaluation of measurement results, as well as an elaborate comparison of models.

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Large Signal Switching Model of GaAs MESFETs

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VERY LOW NOISE 0.20 μm GATE LENGTH GaAs MESFET

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We have fabricated GaAs MESFET with 0.20 μm gate length which have excellent microwave performances. Very low noise figures have been obtained ; these measurements are compared in Fig. 1 to the best reported one, for 0.25 μm GaAs MESFET, GaAlAs/GaAs HEMT, and AlInAs/GaInAs HEMT, as published in 1988 (1-3).

The measured minimum noise figures and associated power gains are as follows :

f (GHz)	12	17	26.5	40
F _{min} (dB)	0.6	0.8	1.3	1.9
G _{ass}	12	11	9	6.5

Our 0.20 μm MESFET have appreciably lower noise figures than the 0.25 μm MESFET ; below 30 GHz, they are practically at the same level as for conventional HEMT.

Lower noise figures result from the reduction of gate length, minimization of access resistances and parasitic capacitances. Two patterns have been designed for short gate length transistors, in order to reduce all the parasitics, especially source inductance, test gate width: 30 μm). Direct write, electron beam lithography is used for the definition of both gate and drain-source contacts ; this gives us an accurate control of the gate length (0.20 μm), the drain-source spacing (1.0 μm), and the position of the gate between the drain and source contacts (centered, in the case of the microphotograph of Fig. 3). Our equipment (Thomson EPG102) would allow us to test even shorter gate lengths, and decentered gates .

TiAu has been preferred to TiAl for the gate metal, in order to reduce the gate resistance ; the measured static gate resistance is about 900 Ω/mm instead of 1900 Ω/mm . The electric characteristics of the Schottky contact is very good in spite of the high doping level of the channel ($6 \cdot 10^{17} \text{cm}^{-3}$).

Conventional AuGeNi ohmic contacts are deposited onto a highly doped ($2 \cdot 10^{18} \text{cm}^{-3}$) GaAs contact layer, and keep an excellent morphology after alloying (see Fig. 3). The GaAs successive layers (conventional undoped buffer, channel and contact layers) were grown using a MBE Varian GEN2 reactor.

We believe that the gate recess control is of crucial importance, especially to reduce access resistances. A wet etching technique has been established to obtain a deep and steep recess: such a gate recess can be observed in the microphotograph of Fig. 3.

We show in Fig. 4 an example of I-V characteristics of such transistors. The maximum measured transconductance is about 450 mS/mm, at $V_{gs} = 0\text{V}$, for a threshold voltage of about -0.7V.

This technology will be applied soon to both conventional and pseudomorphic HEMT structures.

This work has been partly supported by an ESPRIT programme (E2035).

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BACKGATING EFFECT SENSITIVITY TO MATERIAL PARAMETERS IN HEMT STRUCTURES

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The backgating effect is the most studied parasitic effect since it penalizes the integration of devices on both analog and digital GaAs ICs. After having experimentally characterized this effect in HEMTs, a modelling exercise has been achieved, allowing the access to the sensitivity of the device to the material parameters. During the course of this study it has been demonstrated that the kink effect is the "zero substrate-to-source voltage backgate effect". After a short synthesis of our experimental results, this contribution will emphasize with the modelling of the effects. The main results are given.

Standard HEMT structure : The HEMT structure, described in table 1, is used as a standard all along the study. This structure corresponds to the epilayers growth sequence of the measured devices. Starting from these values a study of the sensitivity of each of the parameters to backgating has been carried-out.

GaAs buffer layer residual doping influence : The p type of the GaAs MBE grown undoped buffer layer is now established. The residual doping level ranges from 10^{15} to $2 \cdot 10^{16} \text{ cm}^{-3}$. The 2 DEG density versus backgate voltage, as a function of this residual doping has been computered.

AlGaAs layer doping influence : The AlGaAs donor layer doping level has a direct influence on the 2 DEG density. The question is: does also the AlGaAs doping level have an influence on the backgating ?

GaAs buffer layer thickness influence : The thickness ranges from .2 to 2 μm . The results show that the zero-backgate-voltage 2 DEG value and its variation are both affected by the thickness of the layer.

Semi-insulating material influence : The standard undoped semi-insulating substrate, used in the previous simulation, is supposed to be the result of $5 \cdot 10^{15} \text{ cm}^{-3}$ acceptors compensated by $5 \cdot 10^{16} \text{ cm}^{-3}$ E_{L2} deep donors. In fact this material is non-intentionally doped and these values are residual densities. They may vary from a wafer to the other. Moreover variations exist over a wafer. To appreciate the influence of such variations, the 2 DEG density versus backgate voltage has been computered for various residual concentration combinations.

Conclusion : From these numerical simulation results, it appears clearly that the backgating effect is closely related to the equilibrium between the GaAs buffer layer and the semi-insulating material. Thus, backgating strongly depends on the GaAs buffer layer thickness together with the residuals of each of these materials. Among the results the sensitivity to the semi-insulating substrate residual concentrations could be critical since the undoped semi-insulating material is known to present non uniformities.

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Parasitic induced carrier-deconfinement in HFET's as studied by temperature dependent device characterisation

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The transconductance g_m in field-effect transistors may be given by:

$$(1) \quad g_m = v C_{gs} / L_G$$

where v is the carrier velocity, C_{gs} is the gate-source capacitance and L_G is the gate length, respectively. Cooling HFET's down to low temperatures an increase of carrier velocity may enhance the transconductance in the order of 40% /1/. However much higher enhancement can be observed if the parasitic source resistance significantly decreases due to the lower 2DEG sheet resistance at low temperatures. This effect can not be described according to eq. 2 where the reduction of effective gate-source voltage drop is taken into account, only:

$$(2) \quad g_{m,int} = g_{m,ext} (1 - R_S g_{m,ext})$$

RF-measurements were performed at room and at low temperatures in the frequency range from 45MHz to 10GHz /2/. The small-signal parameters transconductance g_m and gate-source capacitance were determined from measured s-parameters and are plotted as a function of gate-bias in fig. 1. At low temperatures we examined a strong increase of gate-source capacitance which results in a transconductance enhancement according to eq. 1.

The channel potential at the source-end of the gate is $R_S I_D$. This potential reduces the carrier confinement and thus the gate-capacitance C_{gs} . It works similar to an external negative bias at the gate. The gate-source capacitance decreases, if (cp. fig. 1b) :

- I_D is high at forward gate-bias ($V_{GS} > 0,4V$).
- R_S is high due to the high 2DEG sheet-resistance at room-temperature.

A low source-resistance R_S is the key in order to obtain a high transconductance g_m . However the influence on the rf-performance is little as the gate-source capacitance C_{gs} increases simultaneously. In addition the carrier-deconfinement due to the channel resistance ($R_{gs} I_D$) and the drain bias at the drain-end of the gate is present in any HFET. Therefore the gate-source capacitance C_{gs} does not agree with the gate capacitance C_G deduced from CV-measurements without drain bias.

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HEMT MICROWAVE CHARACTERISTICS AT LOW TEMPERATURES

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Currently, two-dimensional electron gas field effect transistors (TEGFETs, HEMTs or MODFETs) are the best high frequency device for super low noise amplifier applications. By taking account of the improvement by a factor 10 of the carrier dynamics when the temperature is reduced from 300K to 77K, significant improvement of the HEMT performances may be expected. Unfortunately, many parasitic phenomena occur at low temperatures which hinders the full use of this potential. The aim of this work is to try to annihilate these parasitic effects and hence try to evaluate the expected improvement in the characteristics.

The approach has been strictly experimental based upon the characterisation of several transistors with different structures grown by MBE and MOCVD technologies at different temperatures. Classical static and R.F. measurements have been done, then accurate parameters measurements have been made at low temperature which are for our knowledge the first microwave parameters variations published. By using an original method we are able to deduce directly all the small signal equivalent circuit parameters and study their variations with temperature.

We have hence been able to observe that the parasitic effects known as the I-V collapse have had disastrous consequences not only on static behavior but also on microwave performance. We have been able to show, through the realisation of a displaced gate transistor (fig. 1), that the fundamental technological parameter to be acted upon in order to suppress the I-V collapse, is the distance between the gate and the recess corner ; it should be inferior to 0.4 μm .

For transistors which do not exhibit these effects, we have observed significant difference in the evolution of the transistor parameters grown by MBE and MOCVD. Nevertheless, the static extrinsic and the intrinsic transconductances have improved (fig. 2), while only the former method has shown an increase in the microwave transconductance (fig. 3), hence, an improvement in the cut-off frequency reaching 60%. It can be seen that there is a corresponding improvement in the cut-off frequency of h_{21} and of F_m . Figure 4 shows the evolution of the cut-off frequency with temperatures at different device gate lengths.

These elements add to the natural reduction of the noise with temperature resulting in observing noticeably reduced noise figure, for example from 1.5dB at 300K to 0.3dB at 77K.

**Performance of P-type Heterostructure Field-Effect-Transistors
between 300 K and 25 K**

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P-Type Heterostructure-Field-Effect-Transistors (p-HFET) are promising candidates for an application in digital circuits with complementary logic in HFET-technology. The performance of the devices can be improved by cooling down the devices due to an increase of the mobility of both, electrons and holes. A detailed analysis of the properties of p-type devices between 300 K and 25 K was performed. The maximum transconductances of devices with 1.4 μm gate length we achieved were 15 mS/mm at 300 K and 55 mS/mm at 77 K, respectively. The transconductance exceeds 80 mS/mm at 25 K. We observed a long channel device behavior at room temperature, while the velocity saturation is dominating at lower temperatures. The measured saturation velocity exceeds $8 \cdot 10^6$ cm/s at 25 K.

The RF-performance has been investigated, too, indicating cutoff-frequencies f_{MAG} as high as 6 GHz at 120 K and 1.8 GHz at 300 K. The experimental results will be compared to those obtained by simulation following a model after Mimura /1/. A further strong increase in f_{MAG} is to be expected since the capacitances are shown to be only weakly temperature dependent while the transconductance obtained by DC measurements strongly increases below 120 K. The experimental values for the transit frequency f_T are in good agreement with those obtained from the inverse transit time of the holes below the gate. Transit times below 20 ps have to be expected at 77 K and below. Thus digital circuits with low propagation delay times and very low power dissipation are possible.

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Fuj. Sci. Tech. J. 19, 243, (1983)

DEVICE 2

Optimization of Subquarter-Micron-Gate MODFETs for
60-90 Ghz Applications Using 2D Hydrodynamic
Energy Modeling

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Abstract:

This contribution addresses the optimization of subquarter-micron-gate MODFETs based on a developed 2D hydrodynamic energy model [1] that features transient simulation of hot electron transport within these ultrahigh speed devices. Besides, this model includes non-stationary electron dynamics effects (which lead to velocity overshoot and undershoot phenomena), real space transfer, back injection, surface degradation effects as well as the deleterious hot electron trapping mechanisms in deep-level DX-Centers.

This model is exploited systematically to study the effect of varying the technological parameters; namely gate length reduction, increased doping levels, aspect ratio and above all gate-to-edge of recess lengths on optimized device performance. The objective is to conceive low-noise microwave devices operating in frequency ranges that exceeds 60GHz.

We found that unless severe restrictions are imposed on the optimized device structures, no improvement or even deterioration of device performance is observed in place of expected amelioration with advanced sophisticated technologies indispensable to fabricate .1u gate MODFETs, for instance. This degradation usually manifests in soft pinch-off phenomena (large turn-on voltages), transconductance compression, higher output conductance and lesser cutoff frequencies. The optimal device dimensions necessary to avoid these effects, in conventional MODFETs, will be cited.

References:

[1] T.Shawki, G.Salmer and O.El-Sayed; "2D Simulation of degenerate hot electron transport in MODFETs including DX-Center Trapping" Proceedings of the 3rd international conference on simulation of semiconductor devices and processes,(SISDEP-88), Bologna (Italy), sep.1988.

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**Properties of Pseudomorphic MODFETs with Different
In-Molefraction**

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A study is performed to achieve an estimation of the performance of pseudomorphic AlGaAs/InGaAs MODFETs versus the conventional AlGaAs/GaAs MODFETs.

To investigate the high frequency performance of pseudomorphic MODFETs, devices with different In-molefraction and gate lengths between $0.35\mu\text{m}$ and $1.3\mu\text{m}$ have been fabricated and characterized. The results obtained are compared to data obtained from AlGaAs/GaAs MODFETs fabricated with the same geometry.

For our submicrometer gate length devices a multigate FET design with six gate fingers each and unit widths between $10\mu\text{m}$ and $20\mu\text{m}$ is used. To exploit the good adhesion of positive resists to improve the gate recess and to increase the gate cross sectional area, a three layer process has been developed. The lateral gate dimension is defined by direct e-beam writing into a top PMMA layer. The vertical pattern is transferred via reactive ion etching (RIE).

Results of our $1.3\mu\text{m} \times 300\mu\text{m}$ devices show unity current gain cut-off frequencies of $f_T=18\text{GHz}$ for our AlGaAs/GaAs devices and $f_T=20\text{GHz}$ for 5% In-content and $f_T=23\text{GHz}$ for 15% In-content, demonstrating the improved frequency properties with increasing In-content. For submicrometer devices, up to now, data are available for the AlGaAs/GaAs devices that exhibit values of $f_T=40\text{GHz}$.

In the report, results of our submicrometer pseudomorphic devices will be given and critical items influencing the performance of MODFETs will be described and correlated to photoluminescence and transport investigations. Such items are the material perfection, the In-molefraction incorporated in the channel, and the structural design.

Improved Gain Designs of Strained InGaAs/InAlAs HEMT's

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Single channel strained $\text{In}_x\text{Ga}_{1-x}\text{As}/\text{In}_{0.52}\text{Al}_{0.48}\text{As}$ ($x>0.53$) High Electron Mobility Transistors (HEMT's) have shown improved transconductance and cutoff frequency characteristics compared to lattice matched ($x=0.53$) devices. $1\mu\text{m}$ devices with $x=0.65$ have, for example, demonstrated extrinsic transconductance value (g_m) of 590 mS/mm and cutoff frequencies (f_T) of more than 45 GHz. In spite of the high g_m , f_T values, these designs present a high output conductance g_d ($g_m/g_d=5$ instead of 14 for $x=0.53$) and have consequently a lower gain and maximum oscillation frequency; typical f_{max} values for $x=0.65$ are of the order of 46 GHz.

To improve the device characteristics we have performed a systematic design study of double heterojunction devices where an undoped $\text{In}_x\text{Ga}_{1-x}\text{As}$ channel is sandwiched between two N-InAlAs donor layers. This paper presents results obtained with both single and double heterojunction designs and compares their characteristics.

Compared to single heterojunction HEMT's the optimized new design shows a higher percentage of quantum well carrier occupation (85.7% instead of 78.3%), a smaller ground state occupancy (74% instead of 85.7%), and a smaller number of "parasitic" carriers (6% instead of 11.5%). These features result in a much better carrier confinement and low output conductance (lowering by a factor of 3 compared to single channel with $x=0.65$). A high g_m/g_d ratio of the order of 22 was also measured.

$1\mu\text{m}$ long-gate devices showed f_T values of 37 GHz and improved gain characteristics with excellent f_{max} values of 66 GHz. Designs with increased In content and good material morphology are currently explored in order to take full advantage of the strained heterostructure properties.

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**Transport Investigation on Pseudomorphic MODFETs by Magneto
Transconductance and Electron Saturation Velocity
Measurements**

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Pseudomorphic AlGaAs/InGaAs MODFET's have shown great potential in high frequency performance superior to that of the conventional AlGaAs/GaAs MODFET's. The excellent microwave properties MODFET's are mainly attributed to the improved transport properties of the InGaAs represented by the low field mobility, the saturation velocity of the electrons, and the sheet carrier concentration in the active channel. For the analysis and optimization of the device and the material structure, it is therefore important to obtain information of these channel parameters by direct measurements on the completed MODFET device.

To obtain this information, we used two techniques that allow temperature dependent direct measurement of the channel transport properties on the completed MODFET device. The techniques are the magneto transconductance mobility measurement method that allows a detailed gate bias dependent profiling of the low field mobility and sheet carrier concentration in the active channel. This technique exploits the geometrical change in resistance of a current carrying structure that is exposed to a magnetic field perpendicular to the current direction. The other technique used allows the determination of the material and structural specific electron saturation velocity by using DC device measurements.

To investigate the transport properties, pseudomorphic 1.3 μ m gate length MODFET's with In-molefractions of 5%, 15%, and 20% In in the channel have been fabricated, and evaluated. The data are given in the appendix.

S-parameter measurements yielded unity current gain cut-off frequencies of 20 GHz for 5% In, 23 GHz 15% In and 26 GHz for devices with 20% In contents. Comparing these results with the transport parameters demonstrate, that the low field mobility is not that much important for determining the device performance and that moderate values of the electron saturation velocity explain well the frequency performance of the devices.

In the report, the measurement techniques further details of the analysis and new results will be presented.

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TECHNOLOGY 2

STABILITY OF DAMAGE ISOLATION IN GaAs

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Ion bombardment damage isolation is frequently used in fabricating GaAs devices. Commonly used ions include protons, helium, boron and oxygen, and there is a dose for each ion above which the isolation resistance decreases. The thermal stability of the isolation is an important issue which has not been extensively investigated. Data for the recovery of electron concentration obtained recently by the isochronal annealing of proton and carbon bombarded GaAs from 100°C to about 700°C are shown in Figure 1. For both projectiles two recovery stages are apparent. For protons there is a small plateau in the recovery at about 260°C and the electron concentration is relatively unchanged for annealing temperatures above about 400°C. For carbon the first annealing stage extends up to about 340°C and after a small reversal in the direction of the electron concentration change between 340 and 480°C a further decrease in electron concentration occurs between 480 and 700°C. The upturn in both curves above 700°C may be due to the loss of arsenic from the bare samples.

DLTS data have been taken on a proton bombarded GaAs sample before and after annealing for one hour at 250°C in an effort to investigate the difference between the defects in as-bombarded and in annealed GaAs. Typical data are shown in Figure 2. The principal trap which is observed before annealing almost completely disappears after the annealing, whereas a trap which is observed at about 220°C grows in concentration and one of the peaks apparent at higher temperature is largely eliminated by the annealing. Work is in progress to measure samples annealed at still higher temperatures. It should be pointed out that there is probably a significant concentration of traps present before annealing, which would exhibit peaks in the DLTS spectrum below 77 K. These traps are probably removed by the 250°C anneal.

Schottky barrier enhancement on InP using pseudomorphic
GaInP MBE layers

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ABSTRACT

The GaP and GaInP material are used as high gap semiconductors on InP to fabricate Schottky diodes. The devices present excellent electrical properties when the ternary strained layer is below the critical thickness. The best device (0.8 eV barrier height ; 1.14 ideality factor; 0.1 nA reverse current at -1V and over 250V breakdown voltage) is obtained on a sample where 11 Å (4 monolayers) of GaP are used as a high gap material to increase the Schottky barrier height on InP. This device is used to fabricate MSM (metal semiconductor metal) detector on InP and leads to high quantum efficiency.

The Indium Phosphide presents potential properties for high speed electronic applications but due to its low Schottky barrier height (0.43 eV for Au/InP : it cannot be used as a gate in Field Effect transistor (FET) fabrication. The InP material has its Fermi level pinned by the surface traps. The Fermi level position at the surface (ψ_s) stays almost constant and the barrier height ϕ_0 of the Schottky diode on InP is almost independent with the metal work function and can be expressed as $\phi_0 = E_g - \psi_s$ (E_g : Bandgap). To increase the Schottky barrier height since there is no way to avoid surface Fermi level pinning, we have to find a high bandgap semiconductor. The use of an heterostructure made of a high gap on a low gap (InP) material leads to an increase of the Schottky barrier height $\Delta\phi$ equal to the amount of the conduction band offset ΔE_c .

There is not a great number of III-V compounds with bandgap higher than that of InP and with the same lattice constants. Semiconductors with Aluminium as a group III element are to be avoided because of the oxidation of these compounds with the ambient air. The Gallium Phosphide has a bandgap of 2.27 eV at room temperature and presents two interesting properties : 1) It seems that GaP on InP presents a band offset ΔE_g with $\Delta E_c = 0.8 \Delta E_g$ which is a favorable case for Schottky barrier height increase and 2) this material does not present a surface Fermi level pinning. The main problem is the high value of the lattice mismatch between InP and GaP (7.1 %). As it

can be shown by the experimental results, the condition to obtain a good Schottky diode (with high ϕ , $n \approx 1$) is to avoid the deposition of a material with a thickness exceeding the critical thickness. The assumption that $\phi = \phi_0 + \Delta E_c$ in the case of a heterostructure GaP/InP is only valid if there is no tunneling through the high gap material. To avoid tunneling, the thickness of the high bandgap material must be greater than about 50 Å. This condition cannot be fulfilled for GaP because the critical thickness for a material of 7.1% lattice mismatch is about 15 Å. To increase the critical thickness, ternary semiconductors like $\text{Ga}_x\text{In}_{1-x}\text{P}$ material are to be used. The critical thickness of 100 Å is obtained for GaInP with 25 % Gallium content, this material presents a bandgap of 1.57 eV at room temperature.

The samples used in the present experiments are grown by gas source molecular beam epitaxy (GS MBE, where only the group V element is provided by a gas source). The growth temperature is 500°C and two different Indium sources are used for InP and GaInP. The growth begins with a 2 µm thick InP layer Silicon doped to $2 \times 10^{16} \text{cm}^{-3}$ or n type undoped ($\sim 10^{16} \text{cm}^{-3}$), followed by the GaInP strained layer on a semi-insulating InP substrate. The Schottky device is fabricated by evaporating gold in vacuum (10^{-6}Torr) through a metallic mask directly on the GaInP surface. Excellent devices are obtained when the high gap layer thickness is kept below critical thickness (Table 1, Figure 1). But poor properties are observed on sample where the critical thickness is exceeded (Table 1).

X Ga	0	18 %	25 %	100 %	100 %	GaAs
e(Å)		150	100	11	100	100
$E_{g\text{ev}}$	1.35	1.50	1.57	2.27	2.27	1.42
I(-1V)	10µA	7nA	0.3nA	0.1nA	6µA	10µA
ϕ_{meV}	434	640	726	800	510	430
$\Delta\phi_{\text{meV}}$	0	206	292	370	76	0
$\Delta E_{g\text{meV}}$	0	145	216	920	920	70
		Pseudomorphic			relaxed	

Table 1 : EXPERIMENTAL RESULTS :

$\text{Ga}_x\text{In}_{1-x}\text{P}/\text{InP}$

e : is the high gap material thickness

I(-1V) : is the reverse current at -1V

ϕ : is the Schottky barrier height

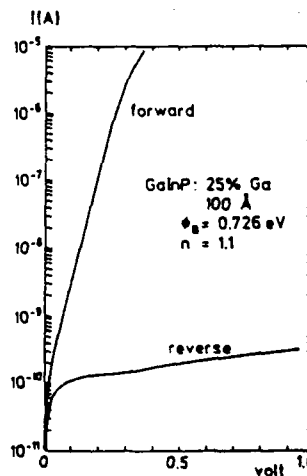


Fig. 1 : I(V) room temperature characteristic of a 0.2 mm diameter Schottky device Au/GaInP/InP with 25 % Ga.

Aspects of high-temperature electronics

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Due to its wide bandgap GaAs is not only of interest for optical, high-frequency and power devices, but also for high-temperature electronics required for example by the machine industry for sensing and control purposes.

We want to report on various aspects of the fabrication of high-temperature reliable circuits. An important factor of the lifetime of devices operating at high temperatures is the degradation of Schottky and ohmic contacts, mainly due to the interdiffusion of Au and Ga. Ohmic contacts with a WSi_x diffusion barrier between the Ge layer (n^+ -dopant in GaAs) and the Au top layer have been examined. The WSi_x was deposited by alternatively evaporating thin layers of W and Si and subsequent annealing. It could be shown that a thin Ni layer on top of the Ge layer enhances the diffusion of Ge into GaAs, thereby increasing the surface doping and reducing the contact resistance. So does an additional very thin Au layer between the Ge and the Ni layers. In both cases, the additional metal must be fully consumed during the diffusion process of Ge to avoid device lifetime problems. A thin Ti layer in the middle of the W-Si sandwich structure enhances the reaction of W and Si to a WSi_x compound, thereby reducing the contact resistance and improving the reliability of the contact. Even without the intermediate Au layer the contact resistance is excellent. The new ohmic contacts were used to produce MeSFETs with TiPtAu gates which did not show any degradation when annealed for 1000 hours at 300°C.

Then we produced a first high-temperature stable IC, namely a differential amplifier. MeSFETs were built with the above technology, interconnections were made of TiPtAu. Nichrome (NiCr) was used for resistors as this material can be made to be very high-temperature stable and to have a very small positive temperature coefficient of the resistance. No change in performance was noted during the first 250 hours of heating at 300°C.

These and similar circuits are very important for intelligent sensors operating at elevated temperatures, preparing the measurement data for a control microprocessor which could be then in a room-temperature environment.

But also the sensing processes should be carefully looked at. In a joint project with mechanical engineers we examined the piezo-electric properties of semiinsulating GaAs at different temperatures. It could be shown that specially Cr compensated (111) material is very suitable for pressure measurements at high temperatures, due to the high resistance of the material. Due to the Cr compensation the intrinsic carriers generated at elevated temperatures are trapped.

"Control of substrate resistivity and implanted Si activation by As overpressure in capless GaAs annealing"

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The thermal stability (or instability...) of GaAs S.I. substrate properties are of primary importance in the production of Si ion implanted GaAs layers for IC's.

In this work we propose our results and interpretation on the control of substrate resistivity as well as Si activation in a capless annealing system using As overpressure.

Semi-insulating undoped ingot annealed and In-doped GaAs LEC wafers were heat treated isothermally in a reactor under different As overpressure conditions ranging from $10E-4$ to 20 torrs.

The increase of As overpressure produced the following results:

- the resistivity variation among annealed and not-annealed samples diminishes (in a different extent) both in undoped and In-doped substrates;

- the average Si activation is increased and the standard deviation of saturation current of closely spaced FET devices is significantly reduced;

- the doping profile tail is sharpened due to a minimized Si indiffusion.

These, and other results, lead to the conclusion that the exodiffusion of EL2 during the annealing is responsible for resistivity changes in GaAs S.I. substrates during annealing in qualitative agreement with the model proposed by Baumgartner. Gallium vacancy indiffusion is also inhibited by high As overpressure determining an increased stability of Si implants. The As overpressure controls the Gallium to Arsenic vacancy ratio over the whole wafer, but the dislocated areas are less sensitive than lower dislocated areas, therefore the level and uniformity of Si activation are controlled by this parameter.

Finally, we think that a variable As overpressure can be used in the annealing of implanted wafers in order to get comparable active layers on GaAs substrates with different electrical properties and dynamical thermal behaviour.

Influence of the sticking layer on the behaviour of ohmic metal contact systems onto n- and p- type $\text{Ga}_{0.47}\text{In}_{0.53}\text{As}$

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In our presentation we want to discuss the metallurgical behaviour of Ag- and Au-based metal systems for ohmic contacts onto GaInAs layers. We will show that the sticking layer is of great importance avoiding metal diffusion into GaInAs.

Therefore different metal systems like Ni/AgZn/Ni, Ni/AgZn/Ti, Ni/AuZn/Ti have been studied by sputtered neutral mass spectrometry (SNMS) /Fig. 1,2/ and TEM investigations /Fig.3/.

On p- GaInAs with a doping level of 10^{18}cm^{-3} the specific contact resistance of all systems investigated is about $10^{-5}\Omega\text{cm}^2$.

Due to the fact that Ti is the better diffusion barrier this material should be favoured in contacting thin p- GaInAs layers.

Furthermore we will present TEM and SNMS investigations of Au-based contacts onto n- GaInAs (see Fig. 4,5,6,7,8,9).

After 900°C RTA annealing of Si- implantation ($E = 100\text{ keV}$, $D = 2 \times 10^{14}\text{ cm}^{-2}$) into n- GaInAs ($n \sim 10^{15}\text{ cm}^{-3}$), we have obtained high surface carrier concentration of about 10^{19} cm^{-3} /Fig.10/. This has resulted in a specific contact resistance $< 10^{-8}\Omega\text{cm}^2$.

This work was supported by Deutsche Forschungsgemeinschaft

THERMALLY ACTIVATED FAILURE MODES AND MECHANISMS OF HEMT's

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Even if HEMTs are replacing GaAs MESFETs for low noise applications, very few data are available concerning reliability and failure mechanisms of these devices. We are running a reliability evaluation plan on both HEMT transistors and low noise MESFET devices for comparison, including different high temperature storage and life tests. We will report here results concerning the first 2500 hours of the thermal storage test at 250 C with no bias applied. Parametric degradation has been followed by monitoring I_{dss} , g_m , V_p and the gate breakdown voltage. Parasitic resistances R_s , R_d and R_g were evaluated by means of "end-resistance" measurements.

HEMT devices from five different suppliers have been submitted to test. Devices mainly differ in gate metallization: pure Al (two suppliers), Al/Ni, Al/Ti, WSi plus Ti/Pt/Au.

Degradation appears to be dominated for shorter times (<500 hours) by interdiffusion/interfacial effects which affect the Schottky contact and/or cause variations in the 2DEG concentration, with consequent degradation of I_{dss} and V_p .

For longer times (>500 hours) increase in R_s and R_d takes place, which gives rise to an increase in R_{on} and is possibly due to ohmic contacts degradation.

Degradation effects at shorter times (<500 hours)

- In pure Al-gate devices, Al/GaAs interdiffusion effects tend to induce both I_{DSS} increase and increase in pinch-off voltage.

- Al/Ti gate devices show a marked increase of gate series resistance R_g (> 300% in 1000 hours!), possibly due to Al-Ti interaction.

- In Al/Ni gate devices a very small decrease in I_{dss} (<5%) takes place, which seems to be directly correlated with an increase of the Schottky barrier height of the gate diode, as obtained by the I-V characteristics.

- Finally, in WSi gate devices no remarkable degradation effect is observed.

Results on low-noise FETs (from the same supplier of Al/Ni HEMTs) show a barrier height increase at short times with no other noticeable effect up to 1600 test hours.

In conclusion we identified different degradation mechanisms affecting both gate region and ohmic contacts; temperature effects on these mechanisms will be investigated by means of other tests at different temperatures.

ASSESSMENT OF COMPOUND SEMICONDUCTOR TECHNOLOGIES
BY SCANNING PHOTOLUMINESCENCE

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The purpose of this contribution is to show the power of scanning photoluminescence measurements for the assessment of the quality and uniformity of compound semiconductor materials.

The results reported here have been obtained with GaAs and InP wafers after such steps as chemical surface treatments, epitaxy (InGaAs and InGaAsP on InP or GaAlAs on GaAs), implantation (Si^{2+} into semi-insulating GaAs and InP substrates), annealing and passivation.

We demonstrate that defects and nonuniformities present in starting wafers and created at the above technological steps can be revealed in fast, non-invasive and contactless way owing to scanning PL measurements.

This concerns in particular dislocations, near-surface defects, doping striations, nonuniform doping activation and modifications of the surface recombination velocity.

In addition, an automatic computing of morphological features on the PL images or an analysis of statistical parameters describing local variations of the PL intensity on the substrate offer new possibilities for the selection of starting and processed wafers at each fabrication stage.

Although further work in this field is still necessary, the results already obtained indicate that scanning PL measurements can be considered as a promising approach for :

- routine "on-line" control and selection of starting and processed wafers after successive technological steps ;

- fast and non-invasive assessment of the processed wafers providing necessary information for the optimization of individual steps.

DEVICE 3

Fast Switching Design of Heterojunction Bipolar Transistors¹

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Heterojunction Bipolar Transistors (HBT's) have in the last years demonstrated promising high frequency operation and high current handling. Carrier transport and switching speed optimization require a careful study of not only the base but also the collector region. The latter permits a higher average velocity by controlling the carrier energy and obtaining better confinement in the Γ -valley. This paper describes such designs based on a steady state and transient Monte Carlo analysis. AlGaAs/GaAs HBT's have also been fabricated and characterized experimentally.

The devices studied are a conventional, an undoped collector and an inverted field HBT. A steady state solution for the electron (Monte Carlo) and hole (drift-diffusion) transport was first obtained by solving self consistently with the potential distribution. Then the base-emitter voltage was turned-off and the collector current transient was evaluated to obtain the storage time and the time (τ) necessary for the electrons to travel through the Space Charge Region (SCR). Shorter transients are indicative of larger overshoot range and average velocity. This is for example the case in special collector designs where the electric field is tailored to vary smoothly in the SCR.

Bias dependent switching studies for $V_{BE} = \text{constant}$ show a τ increase with V_{CE} due to sharper conduction band bending in the SCR and consequently faster transfer to L -valley. Over the entire V_{CE} range, $\tau_{inv.field} < \tau_{und.coll.} < \tau_{conv.}$. For $V_{CE} = \text{const}$ and variable V_{BE} (resulting in I_C variations), τ is found to decrease with I_C due to larger carrier injection into the SCR and E_C band flattening.

Bias dependent microwave measurement of conventional and undoped collector HBT's ($10 \mu\text{m} \times 15 \mu\text{m}$ emitter) showed f_T 's of 5.0 and 7.0 GHz respectively.

The influence of geometrical and material parameters on switching has been studied in view of optimizing each design. Switch-on studies have also been carried out.

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**FABRICATION AND CHARACTERIZATION OF DOUBLE HETEROJUNCTION
GaAlAs/GaAs INTEGRATED INJECTION LOGIC INTEGRATED CIRCUITS**

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GaAlAs/GaAs heterojunction bipolar transistors (HBT's) have demonstrated high speed capabilities (maximum oscillation and cut-off frequencies up to 100 GHz) and are successfully used in digital applications.

Recently results have been reported for GaAs-ECL frequency dividers-by-four with a maximum toggle frequency above 26 GHz (IBM - ISSCC'89).

GaAs - I²L technology with HBT's has also been developed for fabrication of LSI/VLSI circuits with high yields . For example , a 4K gate array and a 32-bit CPU chip with 12,400 gates have been realized by Texas Instruments (ISSCC'88) by implementing Schottky Transistor Logic.

We present the fabrication of a GaAs - I²L ring oscillator : the basic cell is a GaAlAs/GaAs double heterojunction bipolar transistor with a NiCr resistor acting as the current source instead of a pnp transistor .

The thirteen layer structure of the DHBT's is grown by Molecular Beam Epitaxy on a (100) Si-doped GaAs substrate . The emitter - base and collector - base heterojunctions have a graded band gap configuration to avoid spike barriers which can affect the injection and collection of minority carriers . The Al mole fraction and grading width are 0.25 and 800 Å for the emitter and collector regions which are doped with Si to 10^{16} cm^{-3} . The 800 Å GaAs base is doped with Be to 10^{18} cm^{-3} . The P⁺ intrinsic base contact region is formed by multi-implantation of Mg , to maintain a flat doping profile ($\approx 10^{19} \text{ cm}^{-3}$) down to the base layer .

These DHBT's exhibit satisfactory forward and reverse operations (forward and reverse current gains of 500 and 100 are measured) and a very low offset voltage (V_{ce0} 3mV) , which is a basic advantage for a saturated logic such I²L .

A seven-stage ring oscillator is described in a collector-up configuration , with an additional output buffer transistor . For large collector areas ($20 \times 20 \mu\text{m}^2$) , the measured propagation delay time is 850 pS for a power consumption of 1mW per gate.

THE HIGH FREQUENCY PERFORMANCE OF GRADED-BASE AlGaAs/GaAs HBTs

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A comprehensive analytical model of the graded-base AlGaAs/GaAs HBT has been developed and used to examine the factors affecting the high frequency performance of a pyramidal device. Grading of the actual emitter-base junction is also allowed for, using the thermionic and tunnel current representation of Grinberg et al. [1]. In all regions of the device, recombination due to Shockley-Read-Hall, Auger and radiative processes is considered. Inclusion in the model of all these extra current components results in a useful extension of Lundstrom's [2] Ebers-Moll formulation.

The main results of the analysis are:

- (i) the base transit time is a small contributor to the overall delay time. However, its reduction by grading the base does have an impact on f_T and f_{max} . In the baseline device considered here, the presence of base-grading is responsible for an increase in f_{max} of about 15%.
- (ii) the major contributor to the overall delay time, and hence f_T , is the transit time through the collector-base space charge region.
- (iii) by optimizing the basewidth (1500Å) and taking a reasonable upper limit for the base doping density (10^{20} cm^{-3}), and by suppressing the external collector capacitance, an f_{max} of 127 GHz should be attainable.
- (iv) Any significant improvement in f_{max} above this value will require reduction of the extrinsic base resistance, particularly that portion due to the contact resistance.

1. A.A. Grinberg et al., IEEE Trans. Elec. Dev., ED-31, 1758 (1984)
2. M.S. Lundstrom, Solid-State Electron., 29, 1173 (1986)

**Si/SiGe heterojunction bipolar transistors with high current gain
made by molecular beam epitaxy**

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Heterojunction bipolar transistors (HBT's) show great potential for future digital and microwave applications. Impressive results have been achieved with III-V semiconductors, especially in the GaAlAs/GaAs and InP/GaInAs material system.

It is an attractive idea to use a silicon based heterosystem to transfer the advantages of HBT's to the Si technology. Recent progress in the MBE-growth of strained SiGe on Si has now successfully transferred the bandgap engineering to the silicon based system.

A characteristic feature of the Si/SiGe heterosystem is the large difference of the lattice constant. This mismatch produces strain, which strongly influences the band structure (Fig.1). When SiGe is grown onto a Si substrate, the whole difference in the band energy is available as difference in the valence band (Fig.2), resulting in the ideal situation for a hetero bipolar junction. To have a useful transistor, one must still have low recombination currents. This implies a sufficiently defect free hetero interface by avoiding misfit dislocations. For thin SiGe films up to the critical thickness, elastic accommodation prevents the formation of misfit dislocations (Fig.3). The critical thickness is strongly influenced by the growth temperature and the Ge fraction of the SiGe alloy (Fig.4). HBT structures with different base layer thicknesses (40nm to 80nm) and different base doping concentrations up to 10^{19} cm^{-3} were grown by a low temperature MBE process.

Si/SiGe hetero bipolar transistors were fabricated and compared to Si homojunction transistors (Fig. 5). A strain selective etching technique was developed to contact the thin (40nm to 80nm) base layer. To reduce the extrinsic base series resistance, a self aligned technique was applied to bring the base contact close to the emitter contact (Fig. 6). Peak current gain in the range of 200 to 400 were measured for the different heterostructure transistors (Fig.7) compared to a gain of 5 for the homostructure devices.

In the talk, characteristic features of the Si/SiGe hetero bipolar system will be given with respect to the III-V system. The fabrication process and the electrical characteristics will be considered in detail and compared to results obtained with III-V HBT's.

COMPARATIVE MERITS OF AlGaAs/GaAs DMTs AND MULTIPLE HETEROJUNCTION AlGaAs/GaAs HEMTs FOR POWER AMPLIFICATION

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Owing to the recent progress in epitaxial growth techniques, especially by MBE, two AlGaAs/GaAs Field Effect Transistor structures are now offered [1], [2], [3] as alternative to GaAs MESFETs. The former is the DMT and uses a thin heavily doped GaAs channel layer surmounted by an undoped AlGaAs layer just under the Schottky gate. The latter employs a multiheterojunction structure where several undoped GaAs quantum wells are connected in parallel and separated by highly doped AlGaAs supply layers. Both of these structures are presently studied in our laboratory. This paper reports on the results achieved to date with devices having comparable gate dimensions ($L_g \approx 0.5 \mu\text{m}$), and gives first elements of comparison concerning their respective capabilities.

The HEMT structure has been designed with 3 quantum wells and its layers doping and thickness have been optimized in order to obtain high total sheet electron density together with transconductance and cutoff frequency as high and as flat as possible versus the gate-source voltage variations (to ensure power linearity). Two tailoring versions of the upper AlGaAs layer have been tried. One being homogeneously doped and the other pulse-doped, with wide and narrow gate recess in the n^+ cap layer respectively. Typical results of I-V characteristics, transconductance, current gain and maximum available gain (MAG) cutoff frequencies are shown in the joined figures.

The DMT exhibits the possibility of drain current driving up to substantial positive gate-source voltage ($\approx 1.2 \text{ V}$), with no exaggerate gate current, which confirms the ability of the device to operate in accumulation mode. Its saturation drain current is 460 mA/mm and its breakdown voltage about 12 V. In comparison the HEMT offers a slightly lower drain current, 400 mA/mm, for the two versions. But its breakdown voltage depends strongly on the upper AlGaAs layer features: 5 V, in the homogeneous case, despite the wide recess ($2 \mu\text{m}$), and 12 V in the pulse-doped case. The DMT transconductance is excellent with a maximum value of almost 400 mS/mm and a relatively smooth variation over the whole gate source voltage range. The HEMT one does not exceed 220 mS/mm but presents a remarkable flatness versus the gate-source voltage. The HEMT current gain cutoff frequency is of 20 GHz whatever the upper AlGaAs layer features and gate source voltage are. The DMT one is somewhat lower due to an unexpected too high gate source capacitance and is a little less constant versus the gate source bias voltage. Comparable MAG cutoff frequencies are obtained for both devices. The DMT one is 45 GHz. This good result appears to be due essentially to the extremely small values of drain-source conductance ($< 5 \text{ mS/mm}$) and gate-drain capacitance. For HEMT the best result is 42 GHz and corresponds to the narrow recessed structure, which can be explained by its very small access source resistance ($< 0.3 \Omega\text{mm}$).

In conclusion, despite different technological features and physical behaviors, the DMT and the multiple heterojunction HEMT exhibit rather comparable drain current, breakdown voltage and dynamic small signal performance. Both of them appear effectively to be serious candidates to the succession of the GaAs MESFET with a very equilibrate and promising set of characteristics. It remains to examine more accurately what are the consequences of the specific differences of these devices on their respective power performance. Further development of the study will thus focus on this question.

References:

- [1] H. HIDA et al, IEEE, ED34, N° 7, July 1987.
- [2] P. SAUNIER et al, IEEE, EDL-7, N° 9, Sept. 1986.
- [3] K. HIKOSAKA et al, IEEE, EDL-8, N° 11, Nov. 1987.

Microwave properties of $\text{Ga}_{0.47}\text{In}_{0.53}\text{As}$ MISFETs with SiO_2 insulator

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Recent works have demonstrated the high performance of $\text{Ga}_{1-x}\text{In}_x\text{As}$ alloys as channel materials for high speed FETs.

We want to discuss our results of $\text{Ga}_{0.47}\text{In}_{0.53}\text{As}$ MISFETs lattice matched on InP with a pyrolytic deposited SiO_2 gate insulator /Fig. 1/.

Good DC performance of 250 mS/mm and 300 mS/mm has been obtained for devices with gate length of $3\text{ }\mu\text{m}$ and $1.5\text{ }\mu\text{m}$, respectively /Fig. 2/.

The microwave properties show state of the art current gain cutoff frequencies of 6 GHz, 20 GHz and 36 GHz for devices with a gate length of $3\text{ }\mu\text{m}$, $1.5\text{ }\mu\text{m}$ and $0.8\text{ }\mu\text{m}$, respectively /Fig. 3,4/.

In comparison to the $1.5\text{ }\mu\text{m}$ and $0.8\text{ }\mu\text{m}$ gate length device, the MISFET with $3\text{ }\mu\text{m}$ gate length shows higher f_{max} than f_T suggesting that the gate resistance may be causing suppression of f_{max} /Fig. 5/.

The switching behaviour of the $0.8\text{ }\mu\text{m}$ gate length device results in a response time of 52 ps /Fig.6/.

We want to discuss the utility of these MISFETs for digital applications /Fig. 7/.

This work is supported by ESPRIT 927 and 2518

1D simulation and analysis of a three quantum well HEMT.

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We present a 1-dimensional simulation of the DC characteristics for a three quantum well HEMT with two micron gate length. The model developed takes into account the two dimensional Fermi statistics for the calculation of the electron gas densities. The electronic transport in each channel is calculated on the basis on the drift - diffusion model with hyperbolic field dependent mobilities. Current conduction in the doped AlGaAs layer placed between the quantum wells is included. The qualitative validity of the results is confirmed by comparison with experimental measurements. Molecular beam epitaxy was used to grow the layers and optical lithography for device processing. The maximum transconductance measured is 200 mS/mm at room temperature for 1.5 μ m gate length. The model is used to analyse the dependance of the device performance on the layer parameters. The optimization of the transconductance is discussed.

DEVICE 4

Quantitative experimental determination of transient velocity in GaAs.

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A study of non-stationary electron drift velocity in III-V semiconductor compounds has been performed, using photoconduction experiments on planar devices. The analysis of non-stationary transport phenomena consists in a spatial analysis in which results obtained in devices of different lengths are compared. Device lengths range from $0.2\mu\text{m}$, where non-stationary phenomena are preponderant, to a few microns, where stationary transport dominates.

The photocurrent I_{ph} created by photon absorption in the semiconductor is measured between two ohmic contacts deposited on the surface material : it is proportional to $\Delta n \cdot \langle v \rangle$, where Δn represents the photo-electron density which is fixed by the optical generation/recombination mechanisms, and $\langle v \rangle$ is their mean velocity along the device. Δn is kept as small as possible in front of the residual N_D doping level, in order to realize differential small-signal measurements and get rid of contact non-linearities. So as to minimize geometrical effects, the penetration depth is kept as small as possible by an adequate choice of the incident light wavelength : photocurrent lines are located in a well-defined zone under the surface, whose length is close to the interelectrode distance.

The major difficulty for quantitative interpretation of such $I_{\text{ph}}(E)$ experimental results in terms of electron drift velocity variations as a function of the electric field E , lies in the determination of the electron density really created by a given incident photon flux. It depends upon light reflection and diffraction by the thick screen constituted by the metallic electrodes whose distance is only a fraction of the incident light wavelength ($\lambda = 0.633\mu\text{m}$). A diffraction coefficient depending on the interelectrode length has been deduced from the study of the experimental variations of the photocurrent versus the incident light intensity ; it is in good agreement with theoretical calculations performed by O.Mata-Mendez*. $I_{\text{ph}}(E)$ characteristics recorded in devices of different interelectrode lengths have been corrected according to this coefficient and compared quantitatively for the same *absorbed* light intensity.

Modelling of the photoconductive experiment by a bidimensional Monte-Carlo program has been performed, which confirms the correlation between the characteristic shape and the importance of non-stationary transport along the device length.

* O.MATA-MENDEZ, M.CADHILAC, R.PETIT, Jour. Opt. Soc. Am., 73,328,(1983).

Quantitative results are presented for GaAs devices at room temperature. Simulated characteristics are used to fit the electron velocity in a $3\mu\text{m}$ long device at low electric fields. It is experimentally shown that the mean electron drift velocity can reach $3 \cdot 10^7$ cm/s along a $0.2\mu\text{m}$ long GaAs device, submitted to a biasing voltage of 400mV. This value exceeds the stationary electron drift velocity corresponding to this electric field (about 10^7 cm/s for 20kV/cm in GaAs), because of the overshoot effects, which are preponderant along such device lengths. Moreover, the $I_{ph}(E)$ characteristic does not exhibit any saturation for this value of the electric field (20kV/cm), inferring that the mean electron velocity can even increase for higher biasing voltages.

GaInAs Camel Diodes and Camel Transistors Grown by MOCVD

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The camel diode is a majority carrier device where the active region lies far away from the surface of the semiconductor. The device consists of three layers ($n^-p^+n^+$). The thickness of the p^+ sandwich layer is chosen in a way that in thermal equilibrium this layer is fully depleted of free carriers forming a potential barrier in the bulk of the semiconductor. Camel diodes have been realized so far in Si and GaAs, as well as in GaInAs grown by MBE only.

We have fabricated GaInAs camel diodes grown by MOCVD. The doping concentrations are: $N_D^- < 10^{15} \text{cm}^{-3}$, $N_A = 6..8 \cdot 10^{18} \text{cm}^{-3}$, $N_D^+ = 8 \cdot 10^{18} \text{cm}^{-3}$. The thickness of the p^+ -layer varies from 6nm to 12nm giving a potential barrier of 0.3 to 0.65eV. The ideality factor is 1.2 to 1.6. Switching the diode from forward to reverse bias shows no storage time and the fall time is $< 70 \text{ps}$.

The camel transistor consists of two camel diodes back to back. The layers are: $n^-p^+n^+p^+n^-$. The diode with the higher barrier is forward biased. It acts as camel emitter. The other diode is reverse biased, it acts as camel collector. The n^+ layer is the base of the transistor. It must be very thin to allow the ballistic passing of the electrons from the emitter to the collector as hot electrons.

Camel transistors have been fabricated so far in Si and GaAs. We have realized a camel transistor in GaInAs, grown by MOCVD. The barrier height of the emitter diode is 0.55eV, the collector diode has a barrier height of 0.25eV.

The base thickness is 40nm. The base transport factor α is 0.6 at room temperature. Only a weak temperature dependence is observed when the device is cooled down to -170°C .

**Room temperature operation of MOVPE-grown AlGaAs/GaAs
resonant tunneling structures**

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The growth of double barrier quantum wells (DBQWs) for resonant tunneling applications up to now has been a domain of molecular beam epitaxy (MBE). It will be shown that room temperature device operation with good static performance can well be achieved using metalorganic vapour phase epitaxial (MOVPE) layer structures. AlGaAs/GaAs resonant tunneling structures were grown with Al-contents between 40% and 60%, barrier thicknesses of 3nm to 5nm and quantum well width of 4nm and 5nm. Spacer layers of 30nm thickness were used to separate the n-doped contact regions from the nominally undoped DBQWs. Background n-type doping concentrations of less than $1 \cdot 10^{15} \text{cm}^{-3}$ are obtained. TEM analysis shows that the interface abruptness is better than the instrumental resolution of 0.5nm. At room temperature peak current densities of up to $2 \cdot 10^4 \text{A/cm}^2$ and peak-to-valley current ratios of 2.7 are measured for diodes fabricated on these layers. To our knowledge these are the highest values reported so far for MOVPE-grown Al(Ga)As/GaAs DBQWs. Structures of this kind - although not yet optimized - are well suited for QW-devices such as resonant tunneling bipolar transistors (RBT).

INVESTIGATIONS ON RESONANT TUNNELING IN III-V HETEROSTRUCTURES. COMPARISON BETWEEN EXPERIMENTAL DATA AND MODEL CALCULATIONS

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We report experimental data obtained on a set of GaAs/AlGaAs double-barrier resonant tunneling structures in which the thickness of the AlGaAs barriers has been systematically varied from 31 to 7.5 nm.

The resonance width and coherent lifetime change over this range by about eight orders of magnitude. For the thinnest barrier, the resonance lifetime is a few picoseconds, comparable to the mobility (momentum randomization) lifetime.

Our data and their temperature dependencies are compared with characteristics computed from a simple numerical model which solves the Schrödinger's equation for a double-barrier quantum well (DBQW) structure tilted by the applied voltage. Since the model assumes fully coherent tunneling, the comparison with the experimental data particularly stresses the dominance of sequential tunneling in the structures investigated.

Our data point to interface roughness in the well as the possible cause for scattering with non-conservation of the transverse momentum and for the resulting large valley currents. Our best devices exhibit a current peak-to-valley ratio of about 20.

WOSDICE 89, Cabourg

MICROWAVE EVIDENCE OF SUPERLATTICE NEGATIVE
DIFFERENTIAL PERPENDICULAR VELOCITIES IN GaAs/AlAs
SUPERLATTICE STRUCTURES

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We have recently inferred the existence of a bulk negative differential velocity in suitably designed GaAs/AlAs superlattices, from only sublinearities in the d.c. current voltage data of n^+p^- (SL) n^+ structures ¹.

We show here that a double unambiguous confirmation of this assumption is provided by strong resonances in the microwave conductance spectra of such devices, both at the fundamental and at harmonics of the transit-time frequency. True negative differential conductance is obtained or not, and under d.c. or a.c. voltages, depending on the SL thickness and doping level.

Based on these results, we discuss the possibility of high velocity peak to valley ratios, and the high frequency performance of such tunable superlattice oscillators.

1. A. Sibille, J.F. Palmier, C. Minot and F. Mollot, Appl. Phys. Lett. 54, 165 (1989)

Resonant Tunneling between Barrier-Separated 2D Electron Gas Systems

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We have investigated the tunneling processes between two independently contacted two-dimensional electron gas (2DEG) systems. Shifting the two systems energetically with respect to each other, we were able to observe up to eight subband resonances as a series of peaks in the derivative of the tunneling current dI/dV .

By shifting the two systems with respect to each other, a series of subbands can be observed on both sides of the barrier. The current shows a step-like behaviour at every resonance condition, in the first derivative sharp resonances represent tunneling between different 2D subbands. By applying a substrate bias voltage to the inversion layer the subband splittings can be varied over a wide range of energies: for the sample used the splitting between the two lowest subbands can be varied between 8 meV and 30 meV.

In the case of transverse magnetic fields, a new giant splitting of the subband resonances is observed. For $B=1$ T the splitting is 22 meV, which is one order of magnitude larger than the cyclotron energy $\hbar\omega_c$. Below 2 T the splitting shows a linear behaviour versus B . Further, the observed splitting is somewhat larger for higher subband energies. A saturating behaviour is observed at 2.5 T for the lowest subband. The splitting of the higher subband resonances starts to saturate earlier. These effects can be explained using a simple ballistic picture where the canonical momentum of the tunneling electrons is conserved. However, this picture requires ballistic transport from the contact at the top of the sample through a slightly doped n -GaAs layer (800 Å) to the first 2DEG system which is responsible for the momentum selection of the electrons. The second 2DEG system acts only as an analyser. As a proof for this interpretation an applied back-gate voltage does not change the peak-splitting within the experimental accuracy. This picture requires ballistic transport over a distance of 800 Å which is the largest one presently observed.

Double-Barrier Resonant Tunneling Diodes:
Theory and Experiment.

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Abstract

Mounting schemes for DBRT diodes have been developed to obtain stable d.c. characteristics and accurate microwave impedance measurements. A circuit analysis showed that it will be very difficult to stabilize diodes with diameters of more than 30 μm . In agreement with this stable d.c. characteristics could be obtained from diodes of 20 μm diameter.

A careful analysis of the characteristic of $\text{Al}_{0.4}\text{Ga}_{0.6}\text{As-GaAs}$ diodes (barrier width 5.6 nm, well width 5 nm) measured at room temperature showed a perfectly linear behaviour around zero bias voltage and no bistability in the negative resistance region. The characteristic shows a strong asymmetry as regards the peak voltage. Bistability could only be observed in oscillating diodes, so it appears that at room temperature there is no intrinsic bistability in this type of diode.

The d.c. characteristic of the barrier region has been modeled self-consistently using solutions of Schrödinger's equation for rectangular well and barriers and assuming the electron charges to be concentrated in sheets. The model confirms that bistability should not be observed in symmetric barriers. Asymmetric barriers have the possibility of bistability and also show asymmetric characteristics as experimentally observed. The contact regions are modeled using an extended drift-diffusion approach including inertia terms as well as energy-dependent effective mass, mobility and diffusivity, and an equation for energy transport. The two models are matched at the boundaries of the barrier region by requiring continuity of the electric field.

Microwave impedance measurements of diodes with various diameters at bias points in the positive and negative differential resistance regions have been performed up to 18 GHz. The results are matched accurately by a model in which the diode is represented by a capacitance parallel to the d.c. differential resistance, as well as a series loss resistance. Both the capacitance and the parallel resistance scale with the diode area.

CIRCUIT 1

Millimeter Waves

Gallium Arsenide

FECTED-VCO

PRODUCT-DESCRIPTION

FECTED which stands for "field effect controlled transferred electron device" is an active planar IC compatible millimeter wave device capable of amplifying or generating millimeter wave signals in the 50 mW range over wide frequency bands. It is basically a planar gallium arsenide transferred electron device ("Gunn diode") with a MESFET cathode contact which suppresses the usual transit-time-(Gunn-) oscillations. Instead it allows non-transit-time limited operation at high (non-transit-time related) frequencies making it well suited for FM applications. Fabrication is easy as a sub-micrometer semiconductor technology usually needed for the fabrication of conventional planar devices (FETs or HEMTs) operating at 35 GHz is not required. Another important feature is that the gate of the MESFET cathode contact also acts as an "integrated" varactor diode making external circuit matching for VCO-operation very simple.

RESULTS OBTAINED WITH AN ~~MMIC-OSCILLATOR~~ WILL BE PRESENTED AT THE WOCSDICE 89

APPLICATIONS

The new device is well suited and is a cheap source for VCO-applications such as CW-radar operation in distance-gauges or satellite communication receivers.

Information on this device can be obtained from

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15 W Pulsed GaAs PIN- Diodes at Millimetre Waves

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Pulsed power generation in the millimetre-wave region is normally restricted to the application of IMPATT- diodes. However, matching of these devices is rather critical because of the high capacitive current and the relatively low impedance level in IMPATT operation. In contrast, PIN-diodes operated at or near the avalanche frequency should theoretically show relatively high negative resistance with low reactive component. Thus the application of PIN-diodes at mm-wave frequencies seems to be more advantageous as compared to IMPATT-diodes. However, up to this time there are nearly no results reported of PIN- diodes for power generation.

In this paper the fabrication of PIN- diodes is described and measurement results at mm-wave frequencies are given. The initial material for the diodes is fabricated by the help of MBE-technology. The doping concentration of the i-layer is $2 \cdot 10^{13} \text{ cm}^{-3}$ (n-doped), while the highly doped n'- and p'- layers are $2 \cdot 10^{18} \text{ cm}^{-3}$ and $> 1 \cdot 10^{19} \text{ cm}^{-3}$, respectively. The i-zone width of the investigated PIN-diodes is 250 nm. Standard photoresist technology is applied to obtain mesa diodes with different areas from $8 \cdot 10^{-5} \text{ cm}^2$ to $2.4 \cdot 10^{-4} \text{ cm}^2$.

The rf- measurements are carried out using an inductive post waveguide resonator which has been investigated intensively at mm-wave frequencies in this laboratory. The PIN- diodes are operated in pulsed condition with a pulse width of 50 ns - 200 ns and a repetition rate of 50 kHz. Maximum output power of 15 W could be attained at 50.1 GHz. The obtained efficiency of 8 % reaches or even exceeds the maximum efficiency values of conventional pulsed IMPATT- diodes.

FM-Noise Performance of GaAs W-band IMPATT diodes

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GaAs single-drift flat-profile W-band IMPATT diodes were fabricated using a selective etching process with high reproducibility and yield. Typical output power was 270 mW around 94 GHz for diodes with quartz stand-offs and 220 mW with quartz rings /1,2/.

These diodes were tested in a computer assisted noise measurement setup utilizing a quasioptical resonator as FM to AM converter. Mean frequency deviation f_{ms} was measured in a range from 2 kHz to 1.7 MHz off carrier.

As a preliminary result an intrinsic noise measure between 24 dB and 27 dB at medium power levels was determined. These values are clearly below the typical values for Si IMPATT diodes (32 dB) /3,4/ and also below the best values reported from Si single-drift flat-profile diodes. (28 dB) /5/. The corner frequency to the 1/f-flicker-noise was between 100 kHz and 700 kHz.

The single sideband noise to carrier ratio $S/N = -85$ dBc (BW = 1 Hz) at $f_m = 100$ kHz and 20 mW is comparable to Gunn devices in W-band.

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V-Band Microstrip Circuits for GaAs MMIC Application

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The paper describes the investigation of microstrip resonators and power combiners on semiinsulating GaAs substrate for V-band frequencies.

Circular disc and rectangular resonators are the mainly used types in microstrip technology up to mm-wave frequencies. In the case of the circular disc resonator the power generating diode is situated directly in the center of the disc. A tapered output line is coupled via a gap to the disc resonator. For V-band frequencies the disc diameters are between 1.4 and 1.8 mm according to the thickness of the semiinsulating substrate of 200 μm . The second version of the investigated resonators is the rectangular type. Rf power output coupling is achieved by a microstrip line, which is perpendicular to the resonator. The loaded Q-values of the resonators are experimentally found to be about 50. For the monolithical integration of the resonator with an active device, the rectangular type seems to be more advantageous, as in this case via hole etching (for the heatsink) can be obtained from one side instead of etching a hole directly under the disc. Maximum output power of hybrid integrated pulse driven GaAs impatt diodes in the disc resonator is 250 mW at 75 GHz and 80 mW at 70 GHz in the cw condition.

Normally the output power of a single microstrip oscillator is not sufficient and the combination of two or more sources is necessary. Therefore, in this paper two different types of combining circuits are investigated: branchline and ratrace couplers. The measurement results of the investigated couplers have shown that the design of the ratrace couplers is less critical as compared to the branchline couplers. The most remarkable feature of the ratrace coupler is a higher isolation between the ports, necessary to reduce interaction of the sources. Also, a higher combining efficiency is attainable, which is even more important for the application as a power combiner. The combining efficiency of the investigated ratrace and branchline couplers is measured versus frequency. In the frequency range between 59 and 62 GHz an efficiency of more than 90% could be realized.

CIRCUIT 2

Design and Characterization of FETs Picosecond Circuits

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Accurate design and characterization of transistor circuits in the low tens picoseconds require specific approaches to predict and/or measure time domain waveforms precisely. We present selected examples of our recent work in this area applied to NEC710 MESFET: determination of the transistor step response, realization of a picosecond sampling gate, realization of a picosecond step generator. The main features and results of these studies are:

1/ - A very large signal FET model: It is evolved from small signal microwave models. The non linear parameters are described with 2D-look-up numerical tables versus device internal voltages obtained from a full dc and 0.1-18GHz small signal microwave FET characterization (here NEC710). A new approach of parameter extraction is presented where preoptimization is performed sequentially on subsets of parameters contributing to S parameters versus frequency. These preoptimizations improve significantly the final precision of parameter extraction of the channel resistance, the access resistances, the parasitic inductances compared to standard approaches.

2/ - Step response of picosecond FETs: We present the measured and simulated step response of NEC710 (transparency 1). At these time scales, the measuring equipment contributes to the system time response. Simulations take into account all important contributions and use the above large signal model. Figs. 2a and 2b show two cases of measurement of the NEC710 strong signal step response with corresponding bias and drive parameters in Table 2. The amplitude of the drive step is larger in Fig. 2b than in Fig. 2a so that V_{gs} becomes positive and the MESFET Schottky diode strongly clamps the top of the gate signal. The waveshapes are very well reproduced in the simulations and the differences in amplitude and switching times between measurement and simulation do not exceed a few per cent.

We simulate the response of the test card alone driven with a 5ps rise time. The step response at point B of the test card corresponding to the conditions of Fig. 2b is represented in Fig. 3a. The 10-90% switching time of the NEC710 is found to be 20+5ps. Fig. 3a-c illustrates the influence of the parasitic elements of the transistor.

We show in Fig. 4 the influence of the description of the transistor nonlinearities on the accuracy of the time response. The reference is the simulation of Fig. 3a (full line, switching time 20ps). The curves b and c of Fig. 4 show a description with averaged values of non-linear parameters. The current source I_{ds} is always described by a 2-D table. The dashed line corresponds to a description where the three capacitances are represented using a 1-D table as

functions of V_{gs} , each value in the table being averaged over the V_{ds} dependence. Then the switching rise time is 16ps corresponding to a 20% error. The dotted line represents a description where C_{gs} is described with a 1-D table as in curve b and the other capacitances are averaged value over their V_{gs} and V_{ds} dependencies. Now the switching time is 13ps which means an error of 35%.

3/ - A two-stage FET picosecond step sharpener: It uses a NEC710 mounted as shown in Fig. 1 of transparency 2. The Fig. 2 shows the time response at point B to a PPL4100 generator step (4V, 95ps). The measured response is in full line and the simulation (dotted line) includes the response of the instrumentation. The curves from left to right correspond to increasing gate biases V_{gs1} (-1, -2, -3V) with $V_{gs2}=0$: they show that the step sharpener includes a built-in adjustable delay of 17ps/V at $V_{gs1} < -2V$. The adjustment of V_{gs2} to a slightly positive voltage (+0.1V) cleans up the output signal and reduces further the risetime (Fig. 2, left curve), compared to the input step (right curve). A time compression factor of 2.3 (95ps/41ps) is measured. The Fig. 4 shows the simulated intrinsic response (and adjustable delay with V_{gs1} bias) of the step-sharpener which has a 28ps rise time. The step sharpener appears to be a useful tool to investigate the large signal step response of fast transistors.

4/ - Picosecond FET sampling gate: A picosecond GaAs MESFET sampling gate employing a NEC710 as a resistive switch is designed and tested in hybrid technology (Fig. 1 and 2 of transparency 3). Figure 3 shows the time-domain response with a sampling interval of 15.6ps. Curve b is the same signal filtered with a 16ns time constant. The 10-90% transition duration (a and b) is 37ps. A same result is obtained with 3.9ps sampling intervals which show a better resolution than Fig. 3a but could not be memorized in good conditions. The measurement accuracy is +5ps. The Fig. 3c represents the calculated response which takes into account the FET non-linearities, the propagation effects and the SS2 step signal. The simulation of the step response of the NEC710 sampling gate alone gives a 10-90% transition time $t_m = 22 \pm 5ps$. This value compares well with the intrinsic response $t_m = 20 \pm 5ps$ measured in 2/. The excellent agreement between the two types of transition time determinations shows that the sampling gate has an excellent resolution i.e. the aperture time realized by the strobe pulse is much less than 20ps. Figure 4 presents a systematic study (experimental and simulation) of the dynamic of the capture of a single sample selected at the maximum of the input step.

Integrated Laser Driver Circuit Based on
InGaAsP/InP Bipolar Transistors

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Summary:

An integrated laser driver circuit, representing a step towards the monolithic integration of an optical transmitter module, was fabricated on InGaAsP/InP. The laser driver circuit (Fig. 1a) comprises a differential amplifier, consisting of the transistors T_1 and T_3 and a common current source T_2 . The integration of the three bipolar transistors (BT) is simplified by exploiting the invertibility of double-heterostructure BTs. A common epitaxial layer provides the collector for T_2 , operating in normal mode (emitter on top) and the emitter for T_1, T_3 , operating in inverse mode (emitter down). The cross section of the IC, which was fabricated by LPE, is given in Fig. 1b.

The ICs were separated and bonded into 16-lead ceramic chip carriers (Fig. 2a). A test board, based on alumina thickfilm technology, was used for DC- and high-frequency measurements of the IC (Fig. 2b).

Fig. 3 shows the static transfer curves of the integrated laser driver for different values of the external emitter resistance of the current source mode transistor T_2 . The output load resistance is 10 Ω , and the supply voltage 5 V. ECL logic levels at the base terminal of T_1 are sufficient for switching. The current amplification of the IC is > 100 . The highest transconductance achieved is 145 mS.

High frequency operation of the IC was tested by using a differential driving scheme of T_1 and T_3 . Eye pattern diagrams were measured for several bit rates up to 560 Mbit/s (PRBS 2¹⁵-1) one of which is shown in Fig. 4.

Details of the fabrication and function of the integrated laser driver will be given. Enhancement of the upper frequency limit by down-scaled dimensions of the DHBTs retaining the IC fabrication technology and current drive capability, will be discussed.

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Monolithically Integrated BH-Laser/Heterostructure Bipolar Transistor
Combination in the InGaAsP/InP System

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Application of optoelectronic components in communication systems is rapidly increasing in all areas: long haul links, local area (LAN) and computer networks, and even optical chip to chip and intra chip interconnections are considered. To meet the requirements for these highly complex applications, optoelectronic integrated circuits (OEICs) will play a key role. The main driving forces are the demands for very high bitrates, high reliability and low costs of the communication systems.

Compared to microelectronic ICs which tend to employ only one device type to ease fabrication technology, OEICs have to combine electronic and optoelectronic devices with device structures very different from each other.

In this contribution the concept and the realization of a monolithically integrated BH-laser/heterostructure bipolar transistor (HBT) combination will be presented.

The above mentioned problem is solved by application of two new epitaxial technologies: selective epitaxy and deposition of semi-insulating (SI) InP, both by MOVPE. The LPE grown BH-laser structure is regrown by these techniques, so the optical field as well as the charge carriers are effectively confined to the active laser region. The use of SI-InP drastically reduces the parasitic capacitance and yield excellent high frequency performance of $f_{3dB} > 8$ GHz.

The HBT-layer package, consisting of 7 layers with InGaAs base layer and InP emitter and collector layers, is deposited selectively into previously etched recesses in areas between the laser stripes, again by MOVPE. Single HBTs yielded current gain values in excess of $\beta=25.000$. Further, the invertibility, i.e. function when interchanging E- and C-terminals, is demonstrated, too.

The monolithically integrated combination has a mostly planar surface facilitating the fabrication process, and allows for high flexibility for optimizing the different components as well as the circuit concept.

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HEMT MMIC's : A NEW GENERATION OF CIRCUITS

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INTRODUCTION

The development of microwave monolithic circuits, integrated on Gallium Arsenide, has successfully permitted to cover a lot of applications up to 20 GHz. Due to the frequency limitation of the active device, in particular the MESFET, the research in field of new devices is growing to improve the performance of the circuits.

Therefore High Electron Mobility Transistors (HEMT) have been developed at LEP. These transistors, grown by an organometallic chemical vapor deposition technique (MOCVD) are constituted by a heterostructure GaAs/AlGaAs. The HEMT fabricated at LEP with a 0.5 μm gate length exhibits 0.9 dB of noise figure with 9 dB of associated gain at 12 GHz (1), and a typical cut-off frequency F_t better than 35 GHz. The cross section of the transistor is presented figure 1.

Using this new device, first monolithic circuits have been designed and fabricated at LEP, in order to demonstrate : i) the low noise and ii) the high frequencies (up to the millimeter wave range) amplification capabilities.

THE MONOLITHIC AMPLIFIERS

i) the low noise 15 GHz amplifier

The design of this amplifier has been based on accurate electrical models of active and passive elements associated with a detailed characterization of the noise behaviour of the HEMT. To this end, microwave on wafer characterization up to 26.5 GHz has been done.

Figure 2 presents a comparison between the measured and the calculated gain and noise figure. A typical 2.3 dB noise figure with an associated gain of 12 ± 2 dB have been measured over the 13 to 16 GHz frequency bandwidth (2). Figure 3 presents a microphotograph of the circuit. The chip size is 1.5 mm^2 .

ii) the 2 to 42 GHz wide band amplifier

To demonstrate the high frequencies capabilities of the HEMT, an ultra wide band amplifier has been designed with an ambitious gain bandwidth product (6 dB x 42 GHz). A distributed amplifier has been chosen to cover such a bandwidth. Distributed effects along the electrodes of the transistor have been taken into account because the size of the transistor becomes comparable of the wavelength at 40 GHz. To achieve the specifications, a cascode configuration has been used in the amplifier.

Figure 4 presents the measured input and output reflection coefficients and the comparison between the measured and calculated gain responses.

6 ± 1 dB gain with a matching better than 8 dB have been measured from 2 to 42 GHz band. Less than 5.2 dB of noise figure has also been measured up to 18 GHz as shown in figure 5. The microphotograph of the amplifier is shown in figure 6. The chip uses 10 $0.5 \mu\text{m}$ HEMT's and the chip size is 2 mm^2 (3).

The excellent performance in noise figure, gain and frequency obtained with these monolithic circuits using high electron mobility transistors open the way to a new generation of circuits for instance, high performance integrated sub-systems in microwave and millimeter wave ranges. Circuits such as frequency dividers and BPSK modulators operating at 15 GHz, mm-wave oscillators are currently in process.

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IC-internal signal analysis using an e-beam test system
demonstrated on a 1K GaAs SRAM.

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Abstract.

In the conventional cycle of IC development, several redesigns of the circuit are generally required to meet the specifications. This cycle can be shortened by more precisely locating the deviations from the simulations with the help of internal measurements. This aspect becomes more and more important in high-speed GaAs IC's where parasitic elements play a non negligible part. These parasitic elements are introduced unintentionally into the layout and are difficult to simulate accurately. However, internal probing with a HF probe head requires pads large enough to be contacted and is restricted to these locations. It additionally puts a capacitive load on the probed section of the circuit.

The measurements presented here have been realized by means of a high speed e-beam test system developed in our laboratories. It allows for noninvasive measurements on internal signal lines inside a circuit with very high spatial and time resolution.

This e-beam test system has been used to analyse the internal waveforms in a 1K GaAs SRAM. The circuit exhibited an access time of 9.5 ns (simulated value: 7.0 ns) for a power dissipation of 250 mW (measured and simulated). To investigate the causes of the access time discrepancy, a measured time budget for the GaAs SRAM was established for the first time, showing the slower parts of the circuit by comparison with a simulated time budget.

Measured and simulated waveforms have been systematically compared over the circuit. A precise investigation of the read process is presented here. Signal measurements on the bit lines during the read cycle are analyzed.

Conventional access time measurements performed over the cell array are correlated with the previous results giving a consistent explanation of the access time discrepancy in the memory.

This work has been funded by the Federal Department of Research and Technology (NT 2719B) and the EEC (ESPRIT No 843).

A Technology For mm Wave Receiver Components

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A technology for the production of monolithically integrated receivers for application in mm wave radar and communication systems has been developed. The concept is based on the co-integration of high performance schottky diodes with GaAs MESFETs. By using the schottky diodes in the RF mixer and in the frequency multiplier the frequency range up to 100 GHz is covered.

The fully planar process uses B⁺ implantation for the definition of the active areas. A highly conductive buried layer which is important for a very low diode series resistance is obtained by a high dose ion implantation. The n/n⁺ active layer is then epitaxially overgrown using an MOCVD-technique. For the definition of the MESFET gates and the diode fingers an e-beam lithography process which is based on a single layer resist system has been developed. A smallest structure width of 0,3 μm has been obtained. A plasma deposited Si₃N₄ layer is used for passivation and as dielectric layer for the MIM capacitors. The process includes airbridge crossovers and via-holes.

Schottky diode mixers and 4,5 GHz IF amplifiers have been fabricated using this technology. The processing sequence will be described in detail.